# Development Board EPC9042 Quick Start Guide

*300 V Half Bridge with Gate Drive*

## DESCRIPTION

The EPC9042 development board are 300 V maximum device voltage, half bridge with onboard gate drives, featuring the EPC2025 enhancement mode *(eGaN®)* field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2025 *eGaN* FET by including all the critical components on a single board that can be easily connected into any existing converter.

The EPC9042 development board is 2" x 1.5" and contains not only two EPC2025 *eGaN* FET in a half bridge configuration with gate drivers, but also an on board gate drive supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1.

For more information on the EPC2025 *eGaN* FETs please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

**Table 1: Performance Summary (TA = 25°C)**

| SYMBOL | PARAMETER | CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{DD}$ | Gate Drive Input Supply Range | | 7 | 12 | V |
| $V_{IN}$ | Bus Input Voltage Range | | | 240 | V |
| $V_{OUT}$ | Switch Node Output Voltage | | | 300 | V |
| $I_{OUT}$ | Switch Node Output Current | Using EPC2025 | | 3* | A |
| $V_{PWM}$ | PWM Logic Input Voltage Threshold | Input 'High' | 3.5 | 6 | V |
| | | Input 'Low' | 0 | 1.5 | V |
| | Minimum 'High' State Input Pulse Width | $V_{PWM}$ rise and fall time < 10ns | 200 | | ns |
| | Minimum 'Low' State Input Pulse Width | $V_{PWM}$ rise and fall time < 10ns | 500 # | | ns |

* Maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermal cooling.
# Dependent on time needed to 'refresh' high side bootstrap supply voltage.

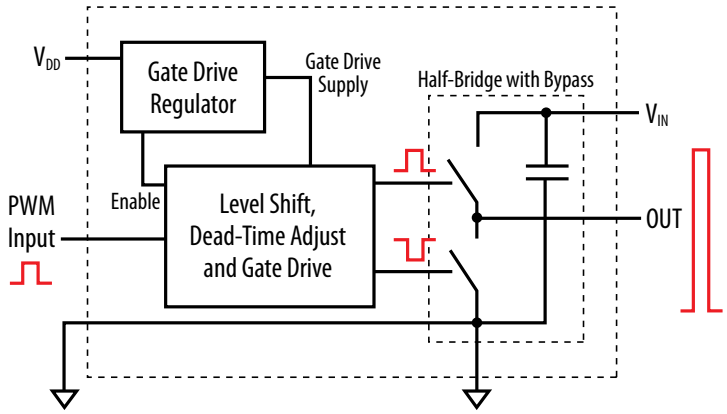


Figure 1: Block Diagram of EPC9042 Development Board

**Demonstration Board Notification**

EPC9042 boards are intended for product evaluation purposes only and are not intended for commercial use. As evaluation tools, they are not designed for compliance with the European Union directive on electromagnetic compatibility or any other such directives or regulations. As board builds are at times subject to product availability, it is possible that boards may contain components or assembly materials that are not RoHS compliant. Efficient Power Conversion Corporation (EPC) makes no guarantee that the purchased board is 100% RoHS compliant. No Licenses are implied or granted under any patent right or other intellectual property whatsoever. EPC assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or any other intellectual property rights of any kind.

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EFFICIENT POWER CONVERSION

## QUICK START PROCEDURE

Development board EPC9042 is easy to set up to evaluate the performance of the EPC2025 *eGaN* FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to $+V_{IN}$ (J5, J6) and ground / return to $-V_{IN}$ (J7, J8).
2. With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required.
3. With power off, connect the gate drive input to $+V_{DD}$ (J1, Pin-1) and ground return to $-V_{DD}$ (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 300 V on $V_{OUT}$ or 240 V on $V_{IN}$)
7. Turn on the controller / PWM input source and probe switching node to see switching operation.
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

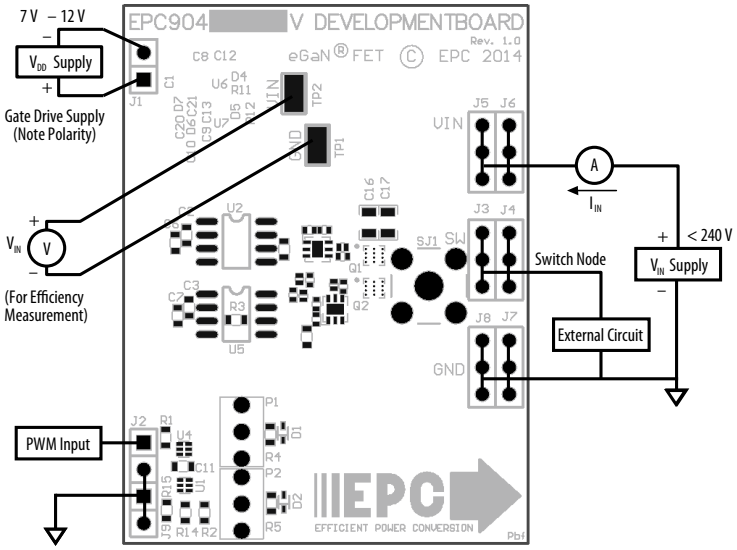



Figure 2: Proper Connection and Measurement Setup

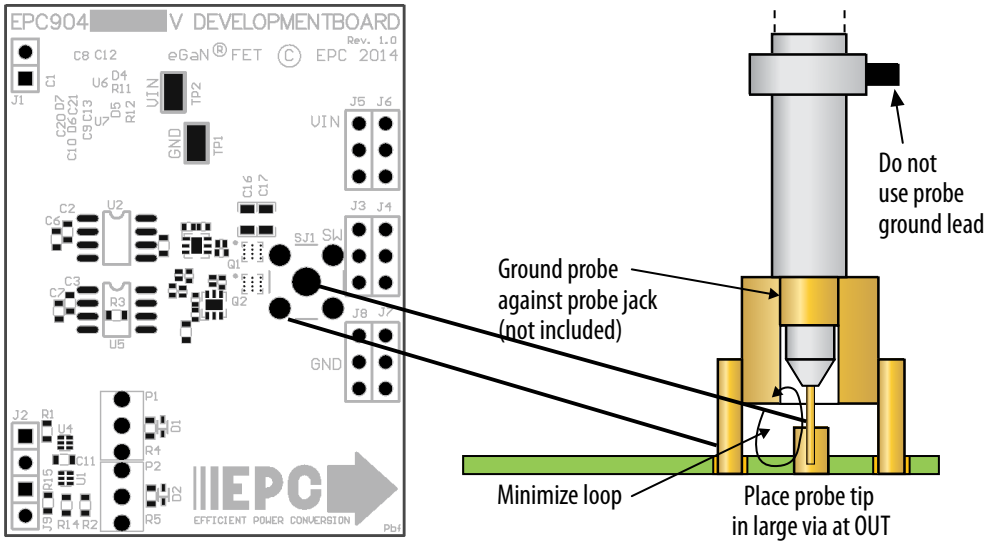



Figure 3: Proper Measurement of Switch Node – OUT

## THERMAL CONSIDERATIONS

The EPC9042 development board showcases the EPC2025 eGaN FET. Although the electrical performance surpasses that for traditional Si devices, their relatively smaller size does magnify the thermal management requirements. The EPC9042 is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.

NOTE. The EPC9042 development boards do not have any current or thermal protection on board.

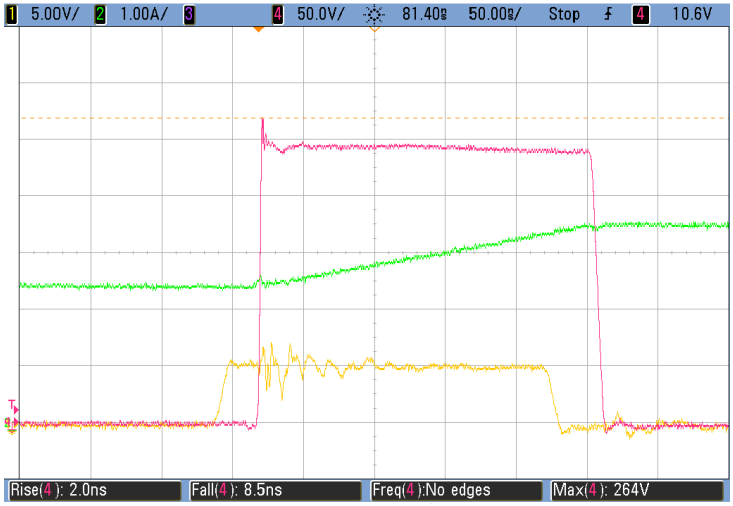
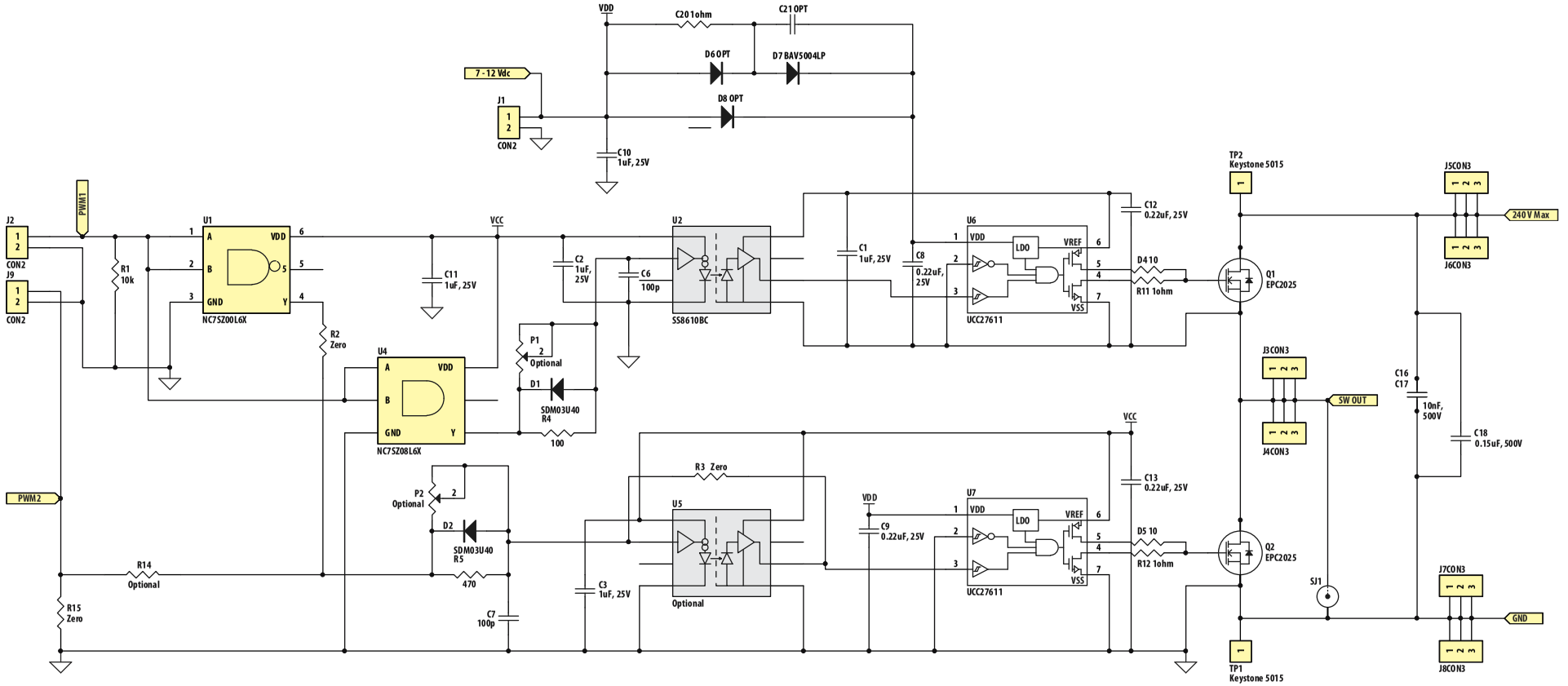



Figure 4: Waveforms for EPC9042, $V_{IN}$ = 240 V to 5 V/ 3 A (100 kHz) Buck converter
CH1: PWM Input – CH2: Inductor current – CH4: ($V_{OUT}$) Switch node voltage

**Table 2 : Bill of Material**

| Item | Qty | Reference | Part Description | Manufacturer / Part # |
|---|---|---|---|---|
| 1 | 5 | C1, C2, C3, C10, C11 | Capacitor, 1uF, 10%, 25V, X5R | Murata, GRM188R61E105KA12D |
| 2 | 2 | C6, C7 | Capacitor, 100pF, 5%, 50V, NP0 | TDK, C1608C0G1H101J |
| 3 | 4 | C8, C9, C12, C13 | Capacitor, 0.22uF, 10%, 16V, X7R | TDK, C1005X7R1C224K |
| 4 | 2 | C16, C17 | Capacitor, 10nF, 10%, 500V, X7R | Kemet, C2012X7T2E104K125AA |
| 5 | 1 | C18 | Capacitor, 0.15uF, 10%, 500V, X7T | Kemet, C1210V154KCRACTU |
| 6 | 2 | D1, D2 | Schottky Diode, 30V | Diodes Inc., SDM03U40-7 |
| 7 | 2 | D4, D5 | Resistor, 10 Ohm, 1%, 1/16W | Stackpole, RMCF0402FT10R0 |
| 8 | 1 | D7 | Diode, 350V | Diodes Inc.,BAV5004LP-7B |
| 9 | 3 | J1, J2, J9 | Connector | 2pins of Tyco, 4-103185-0 |
| 10 | 3 | J3, J4, J5, J6, J7, J8 | Connector | FCI, 68602-206HLF |
| 11 | 2 | Q1, Q2 | eGaN® FET | EPC, EPC2025 |
| 12 | 1 | R1 | Resistor, 10.0K, 5%, 1/8W | Stackpole, RMCF0603FT10K0 |
| 13 | 3 | R2, R3, R15 | Resistor, 0 Ohm, 1/8W | Stackpole, RMCF0603FT00R0 |
| 14 | 1 | R4 | Resistor, 100 Ohm, 1%, 1/8W | Stackpole, RMCF0603FT100R |
| 15 | 1 | R5 | Resistor, 470 Ohm, 1%, 1/8W | Stackpole, RMCF0603FT470R |
| 16 | 3 | R11, R12, C20 | Resistor, 1 Ohm, 1/16W | Stackpole, RMCF0402FT1R00 |
| 17 | 2 | TP1, TP2 | Test Point | Keystone Elect, 5015 |
| 18 | 1 | U1 | I.C., Logic | Fairchild, NC7SZ00L6X |
| 19 | 1 | U2 | I.C., Opto-coupler | Silicon Labs, Si8610BC |
| 20 | 1 | U4 | I.C., Logic | Fairchild, NC7SZ08L6X |
| 21 | 2 | U6, U7 | I.C., Gate driver | Texas Instruments, UCC27611 |
| 22 | 0 | C21 | Optional Capacitor | |
| 23 | 0 | D6, D8 | Optional diodes | |
| 24 | 0 | P1, P2 | Optional potentiometer | |
| 25 | 0 | R14 | Optional resistor | |
| 26 | 0 | U5 | Optional I.C. | |
| 27 | 0 | SJ1 | BNC measurement probe jack | |




# 300V Half-Bridge with Gate Drive, using EPC2025

**Rev 1.1**