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MJD350

High Voltage Power Transistors D-PAK for Surface Mount Applications

- Lead Formed for Surface Mount Applications (No Suffix)
 Straight Lead (I-PAK, "- I" Suffix)



PNP Epitaxial Silicon Transistor

Absolute Maximum Ratings T_C=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V _{CBO}	Collector-Base Voltage	- 300	V
V _{CEO}	Collector-Emitter Voltage	- 300	V
V _{EBO}	Emitter-Base Voltage	- 3	V
I _C	Collector Current (DC)	- 0.5	Α
I _{CP}	Collector Current (Pulse)	- 0.75	Α
P _C	Collector Dissipation (T _C = 25°C)	15	W
	Collector Dissipation (T _a = 25°C)	1.56	W
T _J	Junction Temperature	150	°C
T _{STG}	Storage Temperature	- 65 ~ 150	°C

Electrical Characteristics T_C=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
V _{CEO} (sus)	* Collector-Emitter Sustaining Voltage	$I_{\rm C} = 1 \rm mA, \ I_{\rm B} = 0$	-300		V
I _{CEO}	Collector Cut-off Current	$V_{CB} = -300V, I_{E} = 0$		-0.1	mA
I _{EBO}	Emitter Cut-off Current	$V_{EB} = -3V, I_{C} = 0$		-0.1	mA
h _{FE}	* DC Current Gain	$V_{CE} = -10V, I_{C} = -50mA$	30	240	

^{*} Pulse Test: PW≤300μs, Duty Cycle≤2%

Typical Characteristics

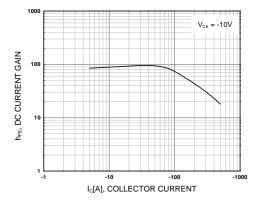


Figure 1. DC current Gain

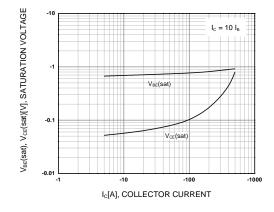


Figure 2. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

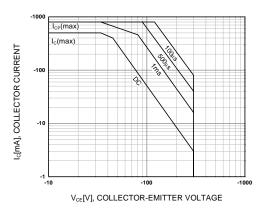


Figure 3. Safe Operating Area

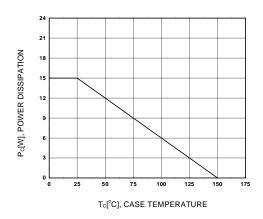
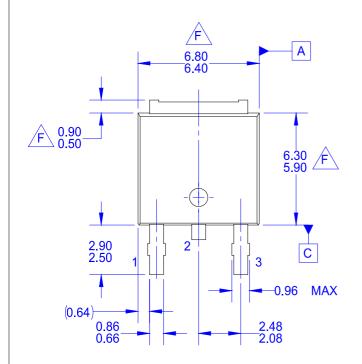
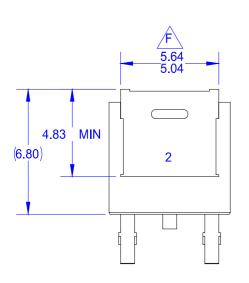


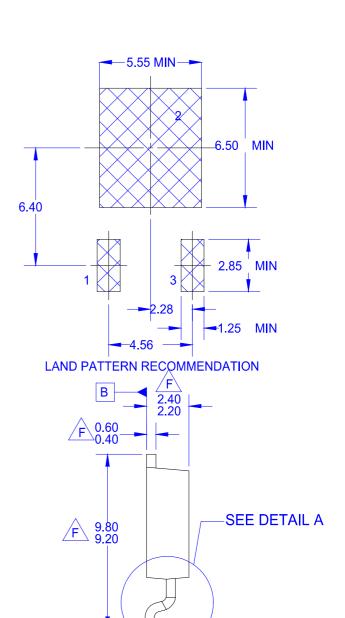
Figure 4. Power Derating

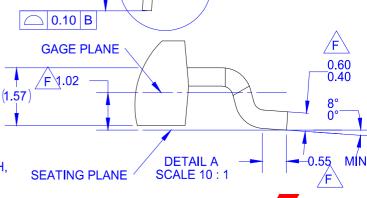




NOTES:UNLESS OTHERWISE SPECIFIED

- A) NOT COMPLIANT TO JEDEC TO-252 VARIATION AB
 B) ALL DIMENSION ARE IN MILLIMETER
 C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- LAD PATTERN PER IPC7351A ATANDARD D) TO228P991X239-3N
- E) DRAWING FILE NAME:MKT-TO252D03REV4.
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