SCOPE: HIGH VOLTAGE, FAULT PROTECTED, ANALOG MULTIPLEXER

Device Type	Generic Number
01	MAX378M(x)/883B
02	MAX379M(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
JE	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
LP	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings

Voltage between Supply Pins ..... +44V
V^+ to GND ..... +22V
V^- to GND ..... -22V
Digital Inputs, Overvoltage :
V_{EN}, V_A (V^+) ..... +4V
V_{EN}, V_A (V^-) ..... -4V
Analog Input with Multiplexer Power On ..... ±65V
(Recommended) V^+ ..... +15V
(Power Supplies) V^-) ..... -15V
Analog Input with Multiplexer Power Off ..... ±80V
Continuous Current, IN or OUT 20mA
Peak Current IN or OUT(Pulsed at 1ms, 10% duty cycle max) 40mA
Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
16 lead CERDIP(derate 10.0mW/°C above +70°C) 800mW
20 lead LCC (derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
Case Outline 16 lead CERDIP..... 50°C/W
Case Outline 20 lead LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
Case Outline 16 lead CERDIP..... 100°C/W
Case Outline 20 lead LCC ..... 110°C/W

Recommended Operating Conditions.

Ambient Operating Range (T_A) ..... -55°C to +125°C
Supply Voltage Range V^- to V^+ ..... -15V to +15V
V_{AH}, Logic Level High ..... +2.4V
V_{AL}, Logic Level Low ..... +0.8V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V+=+15V, V-=-15V, GND=0V V_{AH}=2.4V, V_{AL}=0.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
SWITCH							
Analog-Signal Range	V_{ANALOG}	V_S=±15V, NOTE 1	1,2,3	All	-15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S =±100µA, V_D=±10V	1 2,3	All		3 4	kΩ
Source-OFF Leakage Current	$I_{S(OFF)}$	V_S =±10V, V_D=±10V, V_{EN}=0.8V	1 2,3	All	-0.5 -50	0.5 50	nA
Drain-OFF Leakage Current	$I_{D(OFF)}$	V_S =±10V, V_D=±10V, V_{EN}=0.8V	1 2,3	01	-1 -200	1 200	nA
Drain-OFF Leakage Current	$I_{D(OFF)}$	V_S =±10V, V_D=±10V, V_{EN}=0.8V	1 2,3	02	-1 -100	1 100	nA
Channel-ON Leakage Current NOTE 4	$I_{D(ON)}$	$V_{S(ALL)}$=V_D=±10V, V_{AL}=0.8V, V_{AH}= V_{EN}=2.4V	1	All	-10	10	nA
			2,3	01	-600	600	nA
			2,3	02	-300	300	nA
Differential OFF Output Leakage Current	I_{DIFF}		1,2,3	02	-50	50	nA
Drain-OFF (with Input Overvoltage)	$I_{D(OFF)}$	V_D=0V, V_S=±60V NOTE 2, 3	1	All		20	nA
			2,3			10	µA
Input Leakage Current (with Overvoltage)	$I_{S(OFF)}$	V_S=±60V, V_D=±10V NOTE 2, 3	1	All		25	µA
Input Leakage Current (Power Supplies Off)	$I_{S(OFF)}$	V_S=±75V, V_{EN}=V0=0V A0=A1=A2=0V or 5V, V^+=V^-=0V	1	All		10	µA
INPUT							
Input Low Threshold	V_{AL}	NOTE 3	1,2,3	All		0.8	V
Input High Threshold	V_{AH}	NOTE 3	1,2,3	All	2.4		V
Input Leakage Current (High or Low)	I_A	V_A=5V or 0V NOTE 4	1,2,3	All	-1.0	1.0	µA
SUPPLY							
Positive Supply Range for Continuous Operation	VOP	NOTE 5	1	All	±4.5	±18	V
Positive Supply Current	I+	V_{EN}=0.8V or 2.4V, A0=A1=A2=0V or 5V	1 2,3	All		0.6 0.7	mA
Negative Supply Current	I-	V_{EN}=0.8V or 2.4V, A0=A1=A2=0V or 5V	1 2,3	All		0.1 0.2	mA

TABLE 1. ELECTRICAL TESTS

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V+=+15V, V-=-15V, GND=0V V_{AH}=2.4V, V_{AL}=0.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
DYNAMIC							
Access Time	t_A	Figure 1	9 10,11	All		1.0 1.5	µs
Break Before Make Delay	t_{ON}-t_{OFF}	V_{EN}=+5V, V_{IN}=±10V, A0, A1, A2 strobed	9 10,11	All	25 5		ns
Enable Delay-On Delay	$t_{ON(EN)}$	Figure 2	9 10,11	All		750 1000	ns
Enable Delay-Off Delay	$t_{OFF(EN)}$	Figure 3	9 10,11	All		500 1000	ns
"OFF Isolation"	$OFF_{(ISO)}$	V_{EN}=0.8V, R_L=1kΩ, C_L=15pF, V=7V_{RMS}, f=100kHZ, NOTE 6	9	All	50		dB

NOTE 1: When the analog signal exceeds -13.5V or -12V, the blocking action of Maxim's gate structure starts. Only leakage currents flow and the channel on resistance approaches infinity.

NOTE 2: Steady-state value is shown. Transient leakage is typically 50µA.

NOTE 3: Guaranteed by other static parameters.

NOTE 4: Digital input leakage is primarily from the clamp diodes. Typical leakage is less that 1nA at 25° C.

NOTE 5: Electrical Chacteristics, such as ON Resistance, will change when power supplies other than ±15V are used.

NOTE 6: Guaranteed but not production tested

FIGURE 1 Access Time vs. Logic Level See Commercial Datasheet.

FIGURE 2 Break Before Make Delay See Commercial Datasheet.

FIGURE 3 Enable Delay. See Commercial Datasheet.

TRUTH TABLE **TERMINAL CONNECTION**

A2	A1	A0	EN	MAX378A ON SWITCH		TERMINAL NUMBER	01 MAX378	02 MAX379	01 MAX378	02 MAX379
X	X	X	0	None			J16	J16	L20	L20
0	0	0	1	1		1	A0	A0	NC	NC
0	0	1	1	2		2	EN	EN	A0	A0
0	1	0	1	3		3	V-	V-	EN	EN
0	1	1	1	4		4	IN1	IN1A	V-	V-
1	0	0	1	5		5	IN2	IN2A	IN1	IN1A
1	0	1	1	6		6	IN3	IN3A	NC	NC
1	1	0	1	7		7	IN4	IN4A	IN2	IN2A
1	1	1	1	8		8	OUT	OUTA	IN3	IN3A
						9	IN8	OUTB	IN4	IN4A
				MAX379		10	IN7	IN4B	OUT	OUTA
	A1	**A0**	**EN**	**ON SWITCH**		11	IN6	IN3B	NC	NC
	X	X	0	None		12	IN5	IN2B	IN8	OUTB
	0	0	1	1		13	V+	IN1B	IN7	IN4B
	0	1	1	2		14	GND	V+	IN6	IN3B
	1	0	1	3		15	A2	GND	IN5	IN2B
	1	1	1	4		16	A1	A1	NC	NC
						17			V+	IN1B
						18			GND	V+
						19			A2	GND
						20			A1	A1

NOTE: Logic "0"=V_{AL}≤0.8V
Logic "1"=V_{AH}≥2.4V

ORDERING INFORMATION:	
MAX378MJE/883B	16 CDIP
MAX378MLP/883B	20 LCC
MAX379MJE/883B	16 CDIP
MAX379MLP/883B	20 LCC

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.