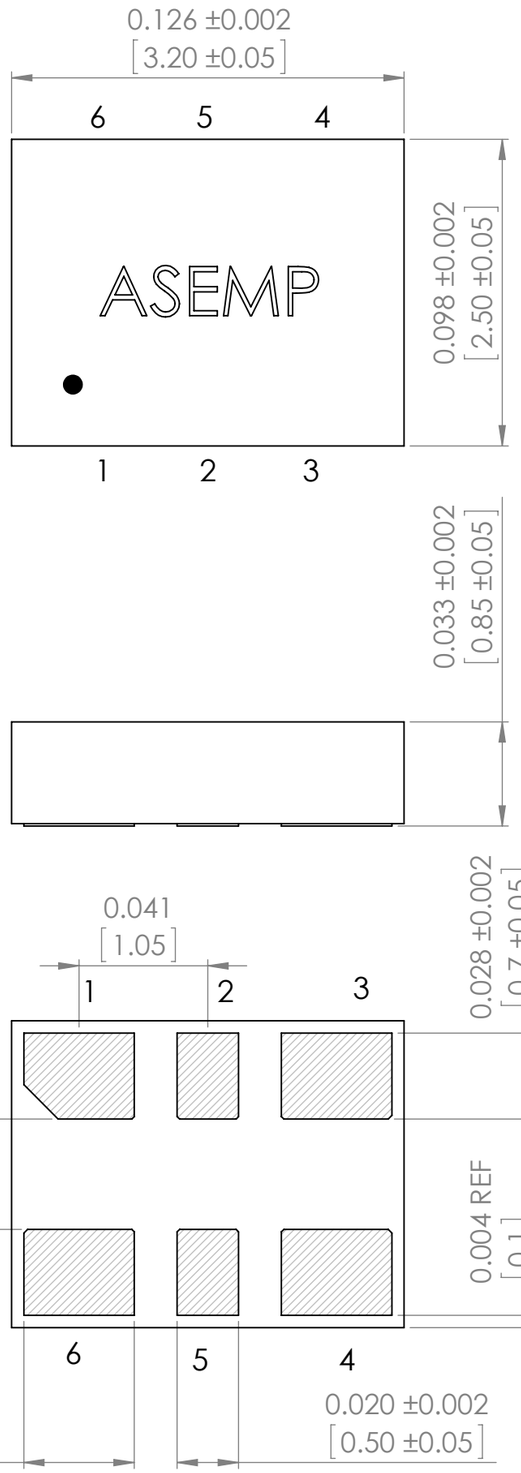
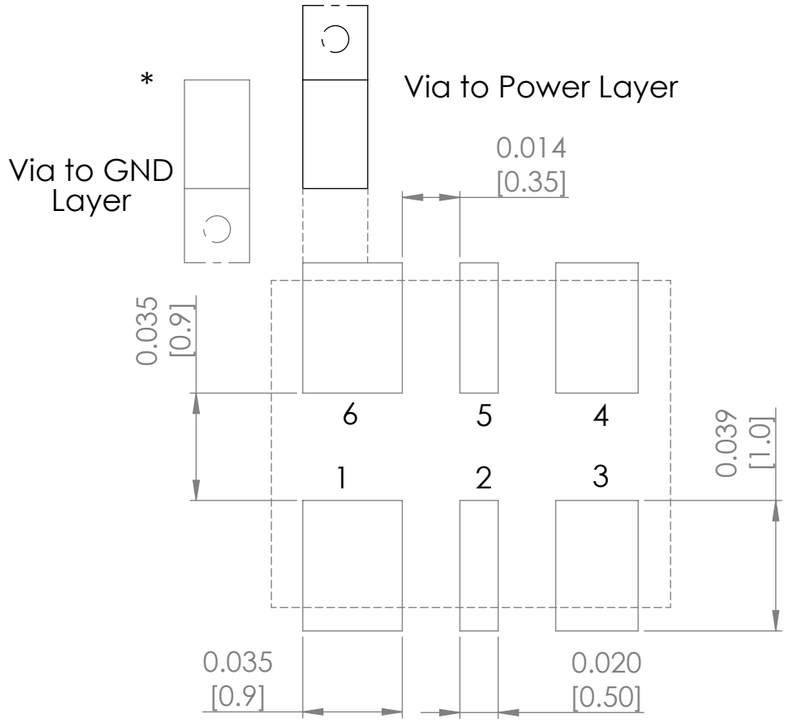
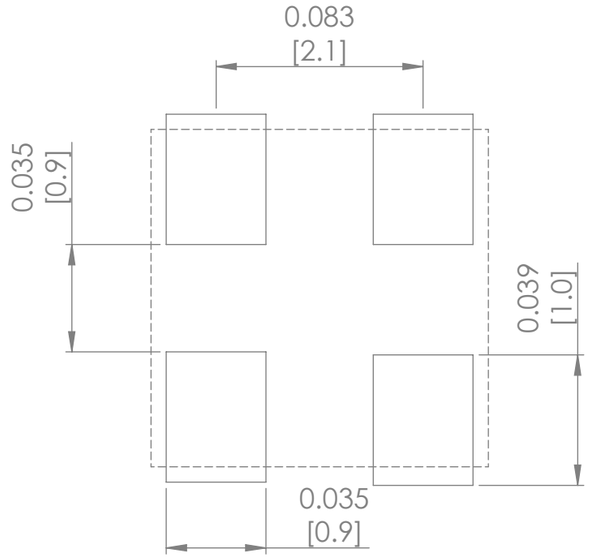


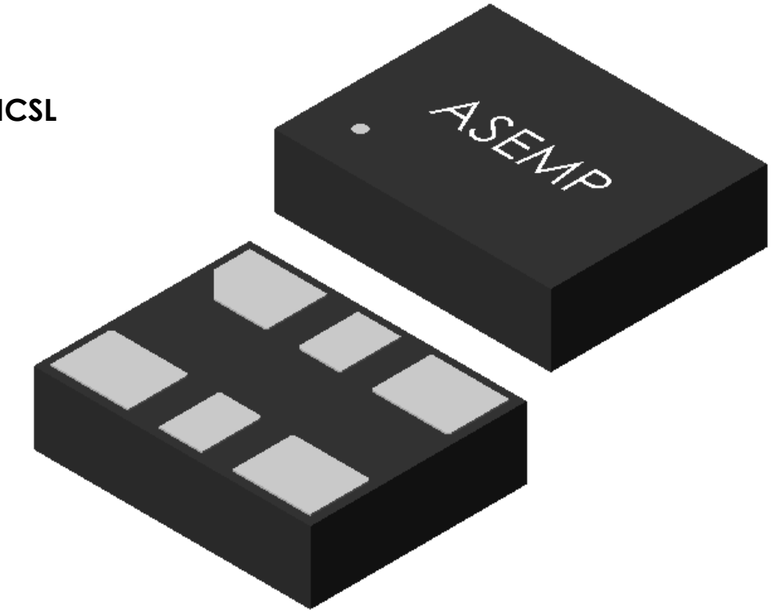


Recommended Land Pattern for LVPECL, LVDS, HCSL



Recommended Land Pattern FOR CMOS

Pin	Function
1	Tri-state
2	NC
3	GND
4	Output
5	NC (CMOS) Output (LVPECL, LVDS, HCSL)
6	Vdd



Note: Recommend using an approximately 0.01uF bypass capacitor between PIN 6 and 3.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCH(MM) SURFACE FINISH: TOLERANCES: LINEAR: ANGULAR:	FINISH:					DEBUR AND BREAK SHARP EDGES
	NAME	SIGNATURE	DATE			
DRAWN	SAAZVAT					
CHK'D	XXXXXX					
APPV'D						
MFG						
Q.A				MATERIAL:		
				WEIGHT:		

DO NOT SCALE DRAWING | REVISION -

ABRACON CORPORATION

30332 Esperanza, Rancho Santa margarita, California 92688

TITLE: OSCILLATOR

DWG NO. ASEMP | A3

SCALE:10:1 | SHEET 1 OF 1