Power Management Switch ICs for PCs and Digital Consumer Products

Power Switch ICs for ExpressCard™

BD4153FV,BD4153EFV

No.10029EBT08

●Description

BD4153FV/EFV is a power management switch IC for the next generation PC card (ExpressCard™) that PCMCIA recommends. Conforms to PCMCIA's ExpressCard™ Standard, ExpressCard™ Compliance Checklist, and ExpressCard™ Implementation Guideline, and obtains the world first Compliance ID "EC100001" from PCMCIA. Offers various functions such as adjustable soft-starter, overcurrent detector (OC function), card detector, and system condition detector, which are ideally suited for laptop and desktop computers.

●Features

1) Incorporates three low on-resistance FETs for ExpressCard™.
2) Incorporates an FET for output discharge.
3) Incorporates an enabler.
4) I Incorporates an undervoltage lockout (UVLO)
5) I Employs SSOP-B24 package.
6) I Employs HTSSOP-B24 package.
7) Incorporates a thermal shutdown protector (TSD).
8) Incorporates a soft-starter.
9) Incorporates an overcurrent protector (OCP).
10) Incorporates an overcurrent flag output (OC).
11) Conforms to ExpressCard™ Standard.
12) Conforms to ExpressCard™ Compliance Checklist.
13) Conforms to ExpressCard™ Implementation Guideline.

●Use

Laptop and desktop computers, and other digital devices equipped with ExpressCard.

●Lineup

Parameter	BD4153FV	BD4153EFV
Package	SSOP-B24	HTSSOP-B24

"ExpressCard™" is a trademark registered by PCMCIA(Personal Computer Memory Card International Association).

●Absolute Maximum Ratings

◎BD4153FV/BD4153EFV

Parameter	Symbol	BD4153FV	BD4153EFV	Unit
Power Supply Voltage	VCC	5.0 *1	5.0 *1	V
Logic Input Voltage	EN,CPPE#,CPUSB#,SYSR,PERST_IN#	5.0 *1	5.0 *1	V
Logic Output Voltage 1	OC	5.0 *1	5.0 *1	V
Logic Output Voltage 2	PERST#	VCC *1	VCC *1	V
Input Voltage 1	V3_IN, V15_IN	5.0 *1	5.0 *1	V
Input Voltage 2	V3AUX_IN	VCC *1	VCC *1	V
Output Voltage	V3,V3AUX,V15	5.0 *1	5.0 *1	V
Output current 1	IOV3, IOV15	2.0	2.0	A
Output current 2	IOV3AUX	1.0	1.0	A
Power Dissipation 1	Pd1	787 *2	-	mW
Power Dissipation 2	Pd2	1025 *3	1100 *4	mW
Operating Temperature Range	Topr	-40～+100	-40～+100	℃
Storage Temperature Range	Tstg	-55～+150	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	+150	℃

*1 However, not exceeding Pd.
*2 Pd derating at 6.3mW/℃ for temperature above Ta=25℃
*3 In the case of Ta≥25°C (when mounting to 70mmx70mmx1.6mm glass epoxy substrate), derated at 8.2 mW/°C.
*4 In the case of Ta≥25°C (when mounting to 70mmx70mmx1.6mm glass epoxy substrate), derated at 8.8 mW/°C.

●Recommended Operating Conditions

◎BD4153FV/BD4153EFV

Parameter	Symbol	MIN	MAX	Unit
Power Supply Voltage	VCC	3.0	3.6	V
Logic Input Voltage 1	EN	-0.2	3.6	V
Logic Input Voltage 2	CPPE#,CPUSB#,SYSR,PERST_IN#	-0.2	VCC	V
Logic Output Voltage 1	OC	-	3.6	V
Logic Output Voltage 2	PERST#	-	VCC	V
Input Voltage 1	V3_IN	3.0	3.6	V
Input Voltage 2	V3AUX_IN	3.0	VCC	V
Input Voltage 3	V15_IN	1.35	1.65	V
Soft Start Setup Capacitor 1	CSS_V3, CSS_V15	0.001	1.0	μF
Soft Start Setup Capacitor 2	CSS_V3AUX	0.001	0.1	μF

* This product is designed for protection against radioactive rays.

●Electrical Characteristics

(unless otherwise noted, Ta=25℃ VCC=3.3V VEN=3.3V V3_IN=V3AUX_IN=3.3V,V15_IN=1.5V)

Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
Standby current	IST	-	35	70	μA	VEN=0V
Bias current 1	Icc1	-	0.25	0.50	mA	VSYSR=0V
Bias current 2	Icc2	-	1.0	2.0	mA	VSYSR=3.3V
[Enable]						
High Level Enable Input Voltage	VENHI	2.3	-	5.5	V	
Low Level Enable Input Voltage	VENLOW	-0.2	-	0.8	V	
Enable Pin Input current	IEN	-	3	10	μA	VEN=3V
[Logic (CPPE#,CPUSB#)]						
High Level Logic Input Voltage	VLHI	2.3	-	VCC	V	
Low Level Logic Input Voltage	VLLOW	-0.2	-	0.8	V	
Logic Pin Input current	IL	-1	0	1	μA	$V_{CPPE\#}$=3.3V or $V_{CPUSB\#}$=3.3V
[Logic (SYSR)]						
High Level Logic Input Voltage	VSYSRHI	2.3	-	VCC	V	
Low Level Logic Input Voltage	VSYSRLOW	-0.2	-	0.8	V	
Logic Pin Input current	ISYSR	6	11	18	μA	V_{SYSR}=3.3V
[Logic (PERST_IN#)]						
High Level Logic Input Voltage	VPSTHI	2.3	-	VCC	V	
Low Level Logic Input Voltage	VPSTLOW	-0.2	-	0.8	V	
Logic Pin Input current	IPST	-18	-11	-6	μA	$V_{PERST\_IN\#}$=0V

●**Electrical Characteristics – Continued**

(unless otherwise noted, Ta=25℃ VCC=3.3V VEN=3.3V V3_IN=V3AUX_IN=3.3V,V15_IN=1.5V)

Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
[Switch V3]						
On Resistance	R_{V3}	-	35	73	mΩ	Tj=-10～100℃ *
Discharge On Resistance	R_{V3}Dis	-	60	150	Ω	
[Switch V3AUX]						
On Resistance	R_{V3AUX}	-	100	210	mΩ	Tj=-10～100℃ *
Discharge On Resistance	R_{V3AUX}Dis	-	60	150	Ω	
[Switch V15]						
On Resistance	R_{V15}	-	42	85	mΩ	Tj=-10～100℃ *
Discharge On Resistance	R_{V15}Dis	-	60	150	Ω	
[Soft Start]						
Charge current	Ichr	1.0	2.0	3.0	μA	
SS_V3 High Voltage	SS_V3high	V3+4	V3+5	V3+6	V	
SS_V15 High Voltage	SS_V15high	V15+4	V15+5	V15+6	V	
SS_V3AUX High Voltage	SS_AUXhigh	1.5	1.8	2.1	V	
Discharge current	IDis	0.3	1.0	-	mA	Vss=1V
Low Voltage	SSLOW	-	-	50	mV	
[Over Current Protection]						
OC Flag V3	OCPV3_S	1.0	-	-	A	
V3 Over current	OCPV3	2.0	-	-	A	
OC Flag V3AUX	OCPV3AUX_S	0.25	-	-	A	
V3AUX Over current	OCPV3AUX	0.50	-	-	A	
OC Flag V15	OCPV15_S	0.50	-	-	A	
V15 Over current	OCPV15	1.20	-	-	A	
OC_Delay Charge current	$I_{OCP\_Delaych}$	1.0	2.0	3.0	μA	
OC_Delay Discharge current	$I_{OCP\_Delaydis}$	1.0	2.0	-	mA	VOC_DELAY=1V
OC_Delay Standby Voltage	VOCP_Delayst	-	-	50	mV	
OC_Delay Threshold Voltage	VOCP_Delayth	0.6	0.7	0.8	V	
OC Low Voltage	VOCP	-	0.1	0.2	V	IOC=0.5mA
OC Leak current	IOCP	-	-	1	μA	VOC=3.65V
[Under Voltage Lockout]						
V3_IN UVLO OFF Voltage	VUVLOV3_IN	2.80	2.90	3.00	V	sweep up
V3_IN Hysteresis Voltage	⊿VUVLOV3_IN	80	160	240	mV	sweep down
V3AUX_IN UVLO OFF Voltage	VUVLOV3AUX_IN	2.80	2.90	3.00	V	sweep up
V3AUX_IN Hysteresis Voltage	⊿VUVLOV3AUX_IN	80	160	240	mV	sweep down
V15 UVLO OFF Voltage	VUVLOV15	1.25	1.30	1.35	V	sweep up
V15 Hysteresis Voltage	⊿VUVLO15	50	100	150	mV	sweep down
VCC UVLO OFF Voltage	VUVLOVCC	2.80	2.90	3.00	V	sweep up
VCC Hysteresis Voltage	⊿VUVLOVCC	80	160	240	mV	sweep down

* Design Guarantee

●Reference data

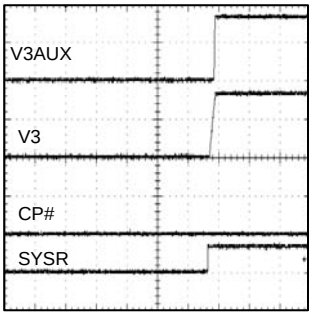


Fig.1 System Stand-by→Active
(Card)

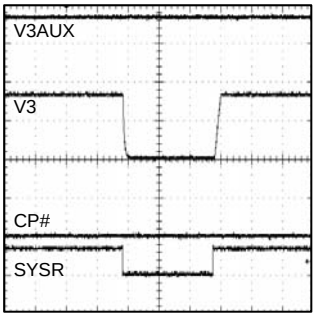


Fig.2 System Active⇔Stand-by
(Card)

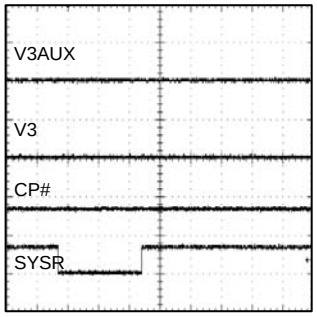


Fig. System Stand-by⇔Active
(No Card)

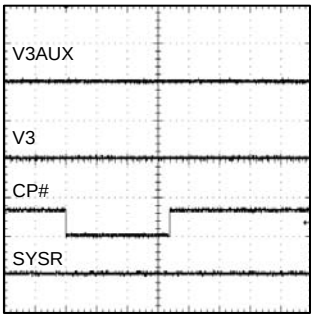


Fig.4 PCI Card Assert/DeAssert
(Stand-by)

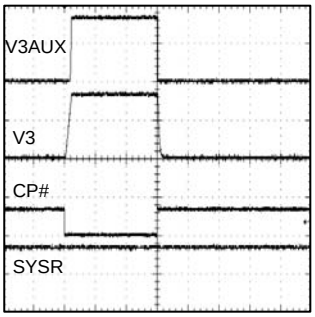


Fig.5 Card Assert/DeAssert
(Active)

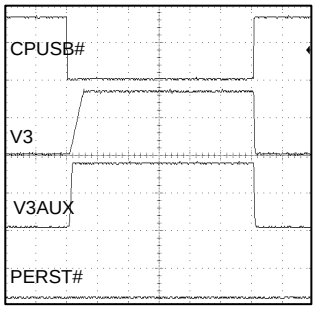


Fig.6 USB Card Assert/ DeAssert
(Active)

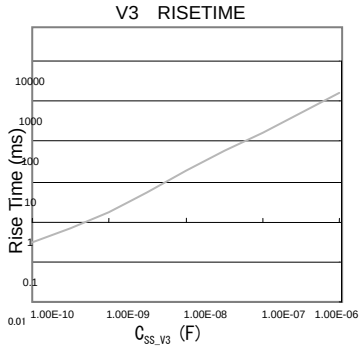


Fig.7 V3 RISETIME

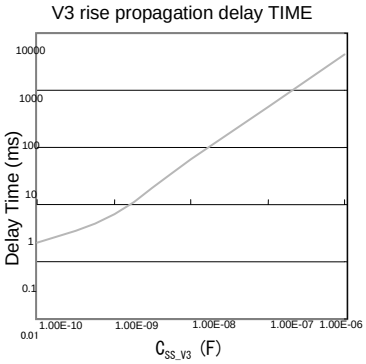


Fig.8 V3 rise
Propagation delay TIME

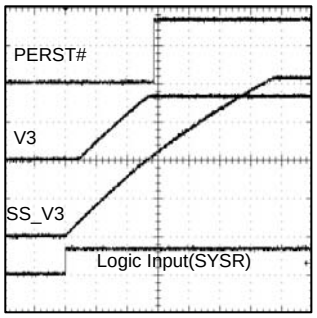


Fig.9 V3 Start up
(Stand-by→Active)

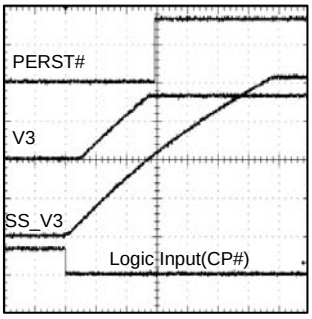


Fig.10 V3 Start up
(Card Assert)

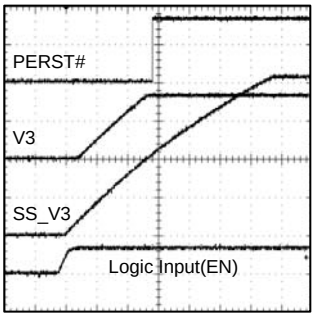


Fig.11 V3 Wave Form
(Shut down→Active)

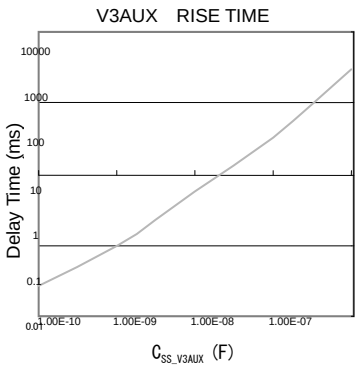


Fig.12 V3AUX
RISE TIME

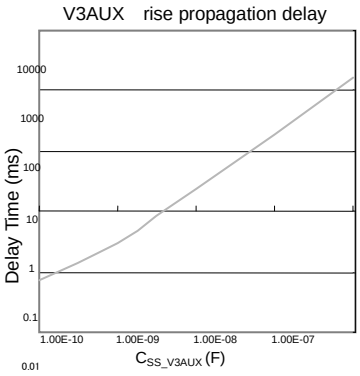


Fig.13 V3AUX
rise propagation delay

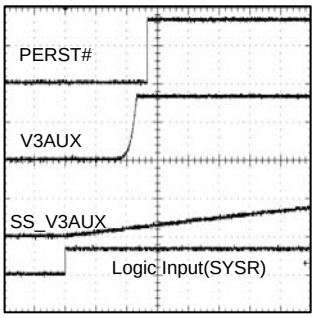


Fig.14 V3AUX Start up
(Stand-by→Active)

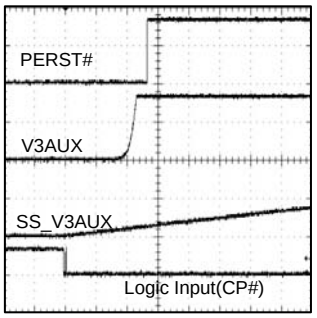


Fig.15 V3AUX Start up
(Card Assert)

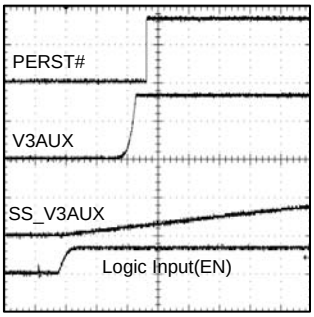


Fig.16 V3AUX Start up
(Shut down→Active)

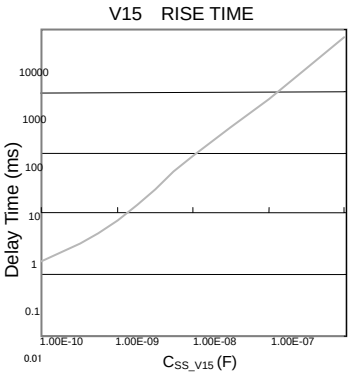


Fig.17 V15 RISE TIME

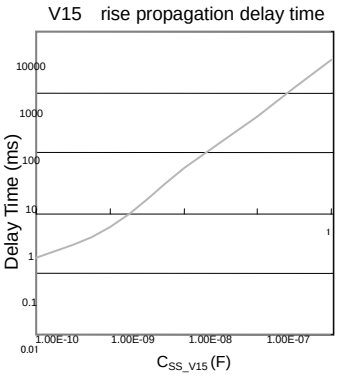


Fig.18 V15
rise propagation delay time

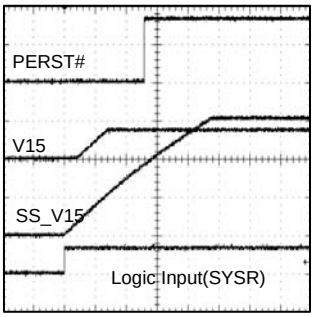


Fig.19 V15 Start up
(Stand-by→Active)

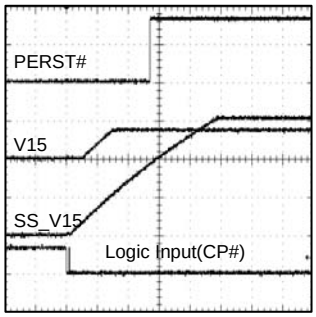


Fig.20 V15 Start up
(Card Assert)

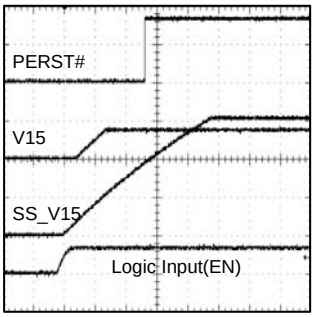


Fig.21 V15 Start up
(Shut down→Active)

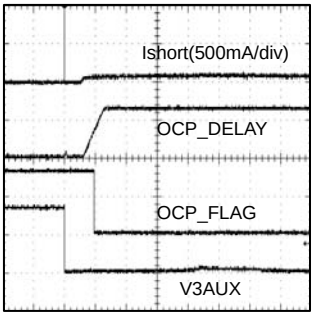


Fig.22 V3AUX Short Circuit

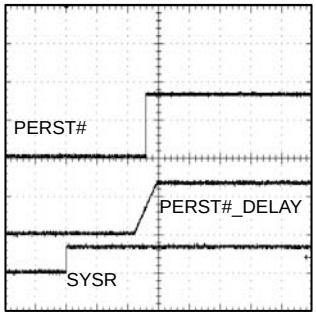


Fig.23 PERST#
L→H Wave Form

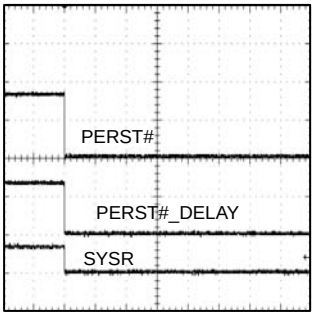
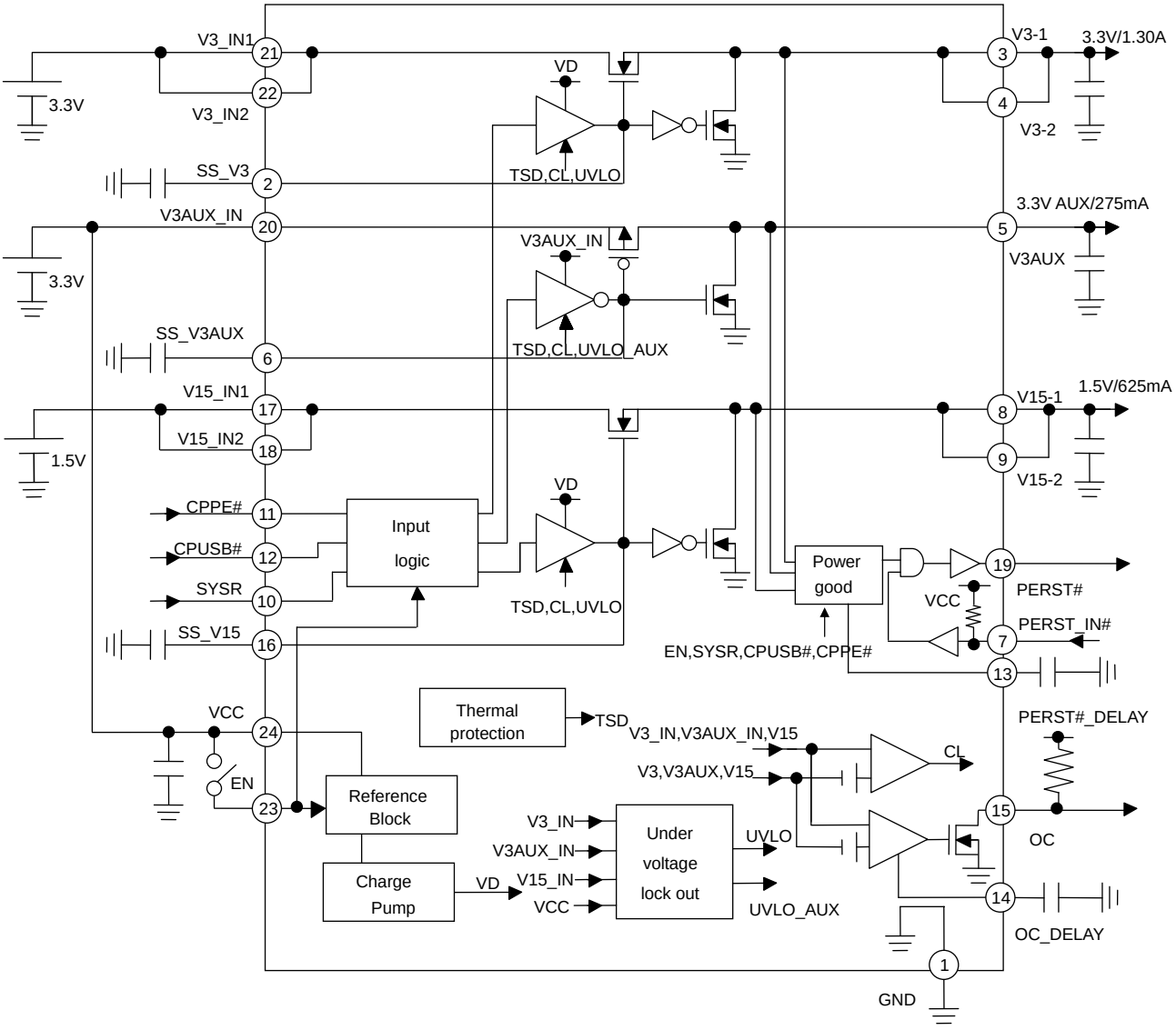
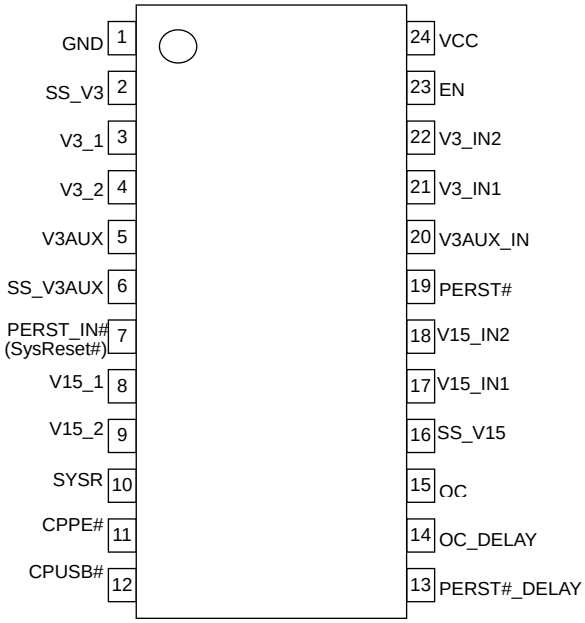


Fig.24 PERST#
H→L Wave Form

●Block Diagram



●Pin Configration



SSOP-B24 Package

●Pin Function

PIN No	PIN NAME	PIN FUNCTION
1	GND	GND pin
2	SS_V3	V3 soft start pin
3	V3_1	V3 output pin 1
4	V3_2	V3 output pin 2
5	V3AUX	V3AUX output pin
6	SS_V3AUX	V3AUX soft start pin
7	PERST_IN#	PERST# control input pin (SysReset#)
8	V15_1	V15 output pin 1
9	V15_2	V15 output pin 2
10	SYSR	Logic input pin
11	CPPE#	Logic input pin
12	CPUSB#	Logic input pin
13	PERST#_DELAY	PERST# delay time setting pin
14	OC_DELAY	OCP delay time setting pin
15	OC	over current protect signal output pin
16	SS_V15	V15 soft start pin
17	V15_IN1	V15 input pin 1
18	V15_IN2	V15 input pin 2
19	PERST#	Logic output pin
20	V3AUX_IN	V3AUX input pin 1
21	V3_IN1	V3 input pin 1
22	V3_IN2	V3 input pin 2
23	EN	Enable input pin
24	VCC	Input voltage

●Description of operations

VCC

BD4153FV/EFV has an independent power input pin for an internal circuit operation in order to activate UVLO, Input logic, and charge pump, the maximum current through which is rated to 2 mA. It is recommended to connect a bypass capacitor of 0.1 µF or so to VCC pin.

EN

With an input of 2.3 volts or higher, this terminal turns to “High” level to activate the circuit, while it turns to “Low” level to deactivate the circuit (with the standby circuit current of 35 µA), discharges each output and lowers output voltage If the input is lowered to 0.8 volts or less.

V3_IN, V15_IN, and V3AUX_IN

These are the input terminals for each channel of a 3ch switch. V3_IN and V15_IN terminals have two pins each, which should be short-circuited on the pc board with a thick conductor. And V3AUX IN terminal should be short-circuited to VCC terminal. Through these three terminals, a big current runs (V3_IN: 1.35A, V3AUX_IN: 0.275 A, and V15_IN: 0.625 A). In order to lower the output impedance of the power supply to be connected, it is recommended to provide ceramic capacitors (of B-characteristics or better) between these terminals and ground; 1 µF or so between V3_IN and GND and between V15_IN and GND, and 0.1 µF or so between V3AUX_IN and GND.

V3, V15, and V3AUX

These are the output terminals for each switch. V3 and V15 terminals have two pins each, which should be short-circuited on the pc board and connected to an ExpressCard connector with a thick conductor as shortest as possible. In order to stabilize the output, it is recommended to provide ceramic capacitors (of B-characteristics or better) between these terminals and ground; 10 µF or so between V3 and GND and between V15 and GND, and 1 µF or so between V3AUX and GND.

CPPE#

The pin used to find whether a PCI-Express signal compatible card is provided or not. Turns to “High” level with an input of 2.3 volts or higher, which means that no card is provided, while it turns to “Low” level when the input is lowered to 0.8 volts or less, which means that a card is provided. Controls turning ON/OFF of the switch according to the status of the system.

CPUSB#

The pin used to find whether a USB2.0 signal compatible card is provided or not. Turns to “High” level with an input of 2.3 volts or higher, which means that no card is provided, while it turns to “Low” level when the input is lowered to 0.8 volts or less, which means that a card is provided. Controls turning ON/OFF of the switch according to the system status.

SYSR

The pin used to detect the system status. Turns to “High” level with an input of 2.3 volts or higher, which means that the system is activated, while it turns to “Low” level when the input is lowered to 0.8 volts or less, which means that the system is on standby.

PERST_IN#

The pin used to control a reset signal to a card (PERST#) from the system side. (Also referred to as “SysReset#” by PCMCIA.) Turns to “High” level with an input of 2.3 volts or higher, and turns PERST# to “High” level AND with a “Power Good” output. Turns to “Low” level and turns PERST# to “Low” level when the input is lowered to 0.8 volts or less.

PERST#

The pin used to provide a reset signal to a PCI-Express compatible card. The status is determined by each output, PERST#_IN, CPPE# system status, and EN on/off status. Turns to “High” level and activates the PCI-Express compatible card only if each output is within the “Power Good” threshold with the card kept inserted and with PERST_IN# turned to “High” level.

PERST#_DELAY

Delay during which the level at PERST# pin turns from Low to High may be set with a capacitor externally applied. The delay time is determined by the regulated current (2 µA), the reference voltage (0.7 volts) inside the IC and the capacitance of the capacitor externally applied. The delay time is specified as “at least 1 ms” in “ExpressCard Standard”. It does not synchronize with PERST_IN#, and it synchronizes only with a “Power Good” output inside the IC. Turns to “Low” level when SW is turned OFF.

OC

Turns its output to “Low” level if an overcurrent condition is detected. This open drain output may be pulled up to 3.6 volts power supply via resistor.

OC-Delay

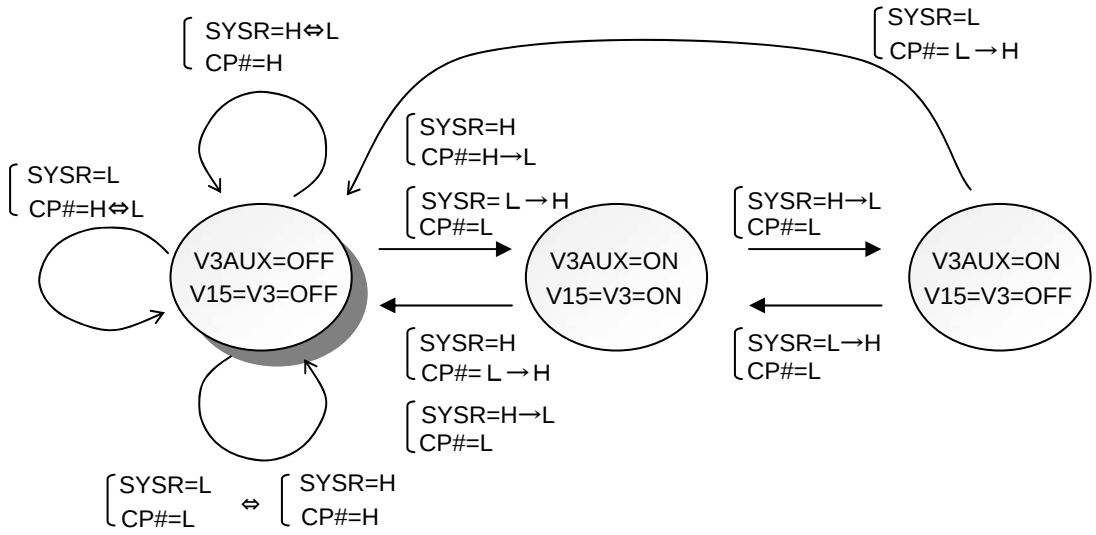
Delay during which the level at OC pin turns from High to Low may be set with a capacitor externally applied. The delay time is determined by the regulated current (2 µA), the reference voltage (0.7 volts) inside the IC and the capacitance of the capacitor externally applied. May be used to control with the OC status fed back to the system. If fed back to EN terminal of this IC, it may be used to turn OFF the output that is provided when an overcurrent condition is detected.

●Timing Chart

Power ON/OFF Status of ExpressCard™

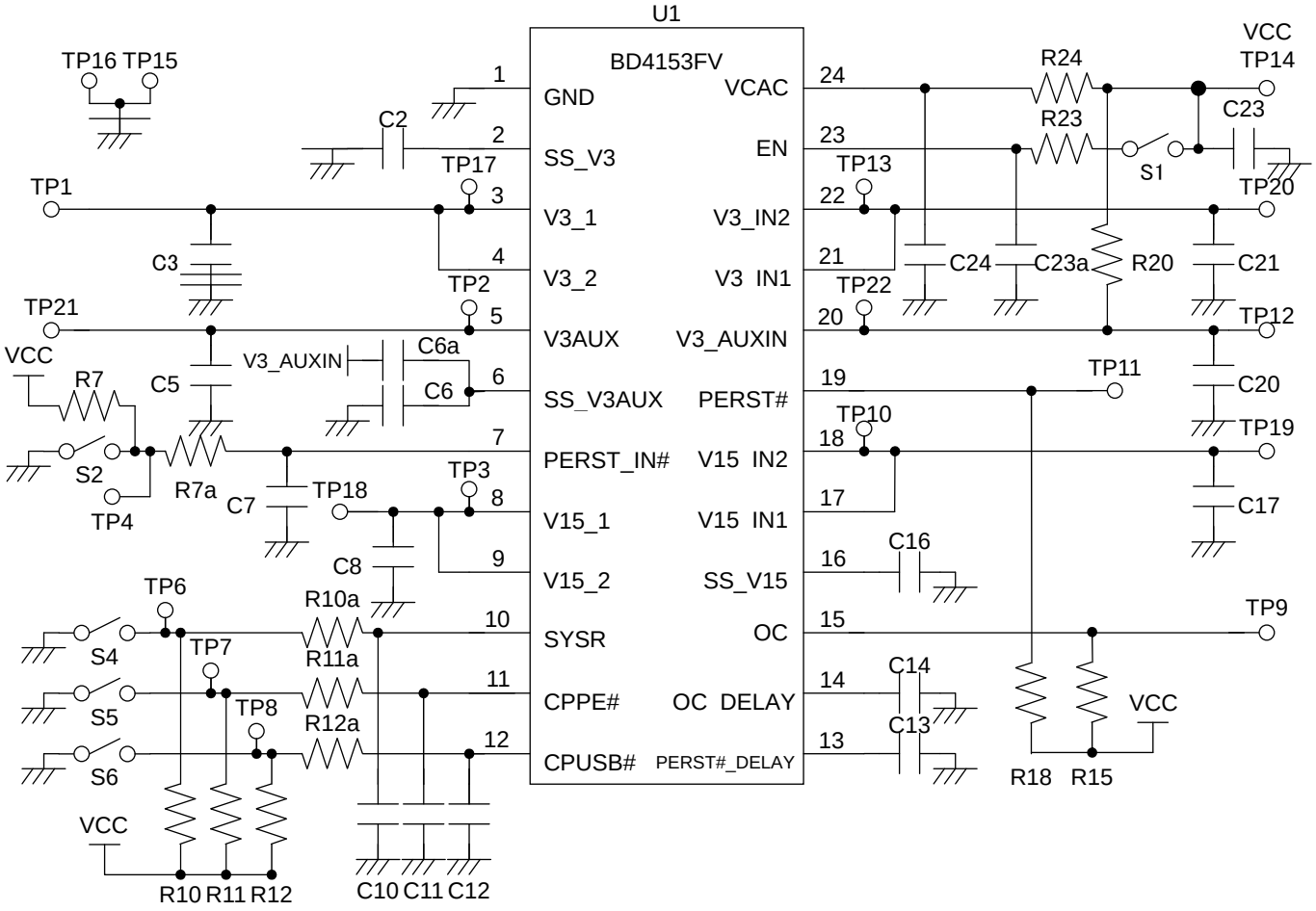
System Status		ExpressCARD™ Module Status	Power Switch Status	
Primary	Auxiliary		Primary	Auxiliary(3.3V Aux)
OFF	OFF	Don't Care	OFF	OFF
ON	ON	De-asserted	OFF	OFF
		Asserted	ON	ON
ON	ON	De-asserted	OFF	OFF
		Asserted Before This System Status	OFF	ON
		Asserted After This System Status	OFF	OFF

ExpressCard™ States Transition Diagram



System Status		Card Status	
Stand-by Status	:SYSR=L	CardAsserted Status	:CP#=L
ON Status	:SYSR=H	Card De-asserted Status	:CP#=H
From ON to Stand-by Status	:SYSR=H→L	From De-asserted to Asserted Status	:CP#=H→L
From Stand-by to ON Status	:SYSR=L→H	From Asserted to De-asserted Status	:CP#=L→H

■ BD4153FV Evaluation Board Circuit



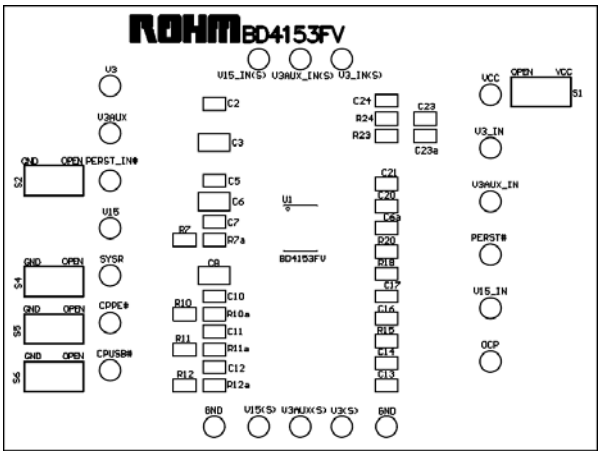
■ BD4153FV Evaluation Board Application Components

Part No	Value	Company	Parts Name
U1	-	ROHM	BD4153FV
R7	10kΩ	ROHM	MCR03series
R10	10kΩ	ROHM	MCR03series
R10a	0Ω	ROHM	MCR03series
R11	120kΩ	ROHM	MCR03series
R11a	0Ω	ROHM	MCR03series
R12	120kΩ	ROHM	MCR03series
R12a	0Ω	ROHM	MCR03series
R15	10kΩ	ROHM	MCR03series
R18	-		-
R20	0Ω	ROHM	MCR03series
R23	0Ω	ROHM	MCR03series
R24	10Ω	ROHM	MCR03series
C2	2200pF	murata	GRM18 series
C3	10μF	murata	GRM21 series
C5	1μF	murata	GRM21 series
C6	0.01μF	murata	GRM18 series

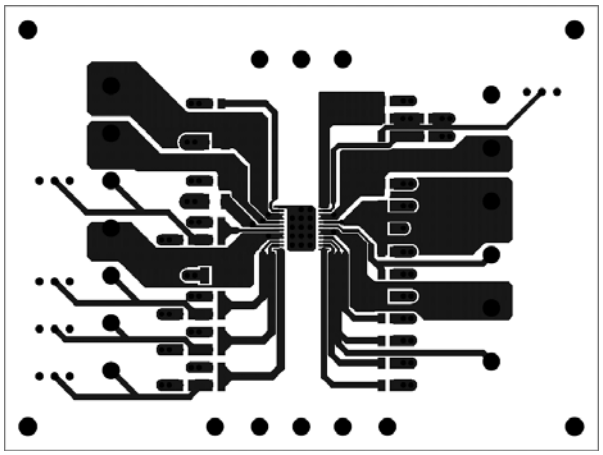
Part No	Value	Company	Parts Name
C6a	-	-	-
C7	-	-	-
C8	10μF	murata	GRM21 series
C10	-	-	-
C11	-	-	-
C12	-	-	-
C13	0.033μF	murata	GRM18 series
C14	0.22μF	murata	GRM21 series
C16	2200pF	murata	GRM18 series
C17	1μF	murata	GRM21 series
C20	0.1μF	murata	GRM18 series
C21	1μF	murata	GRM21 series
C23	0.1μF	murata	GRM18 series
C23a	-	-	-
C24	0.1μF	murata	GRM18 series

■ BD4153FV Evaluation Board Layout

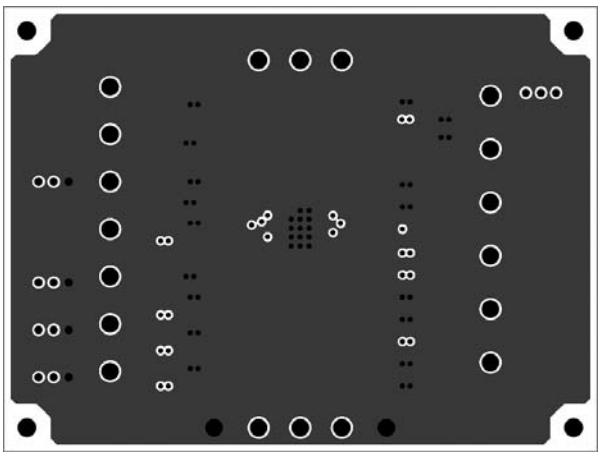
Silk Screen



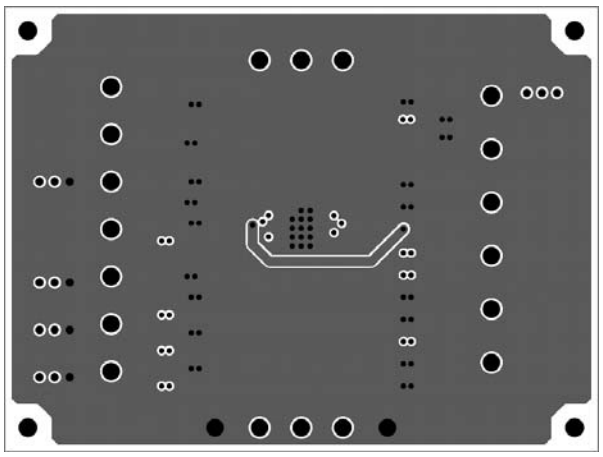
TOP Layer



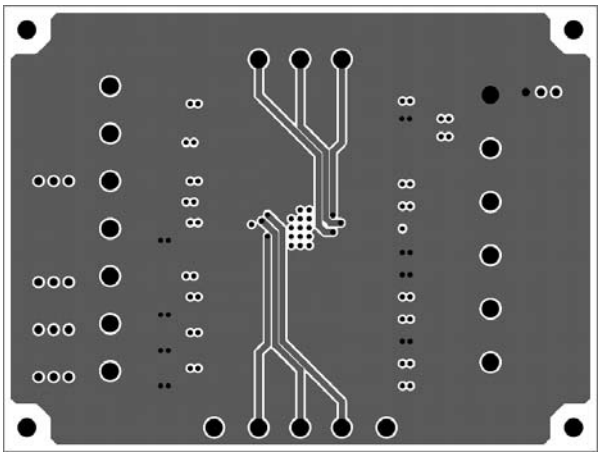
Mid Layer 1



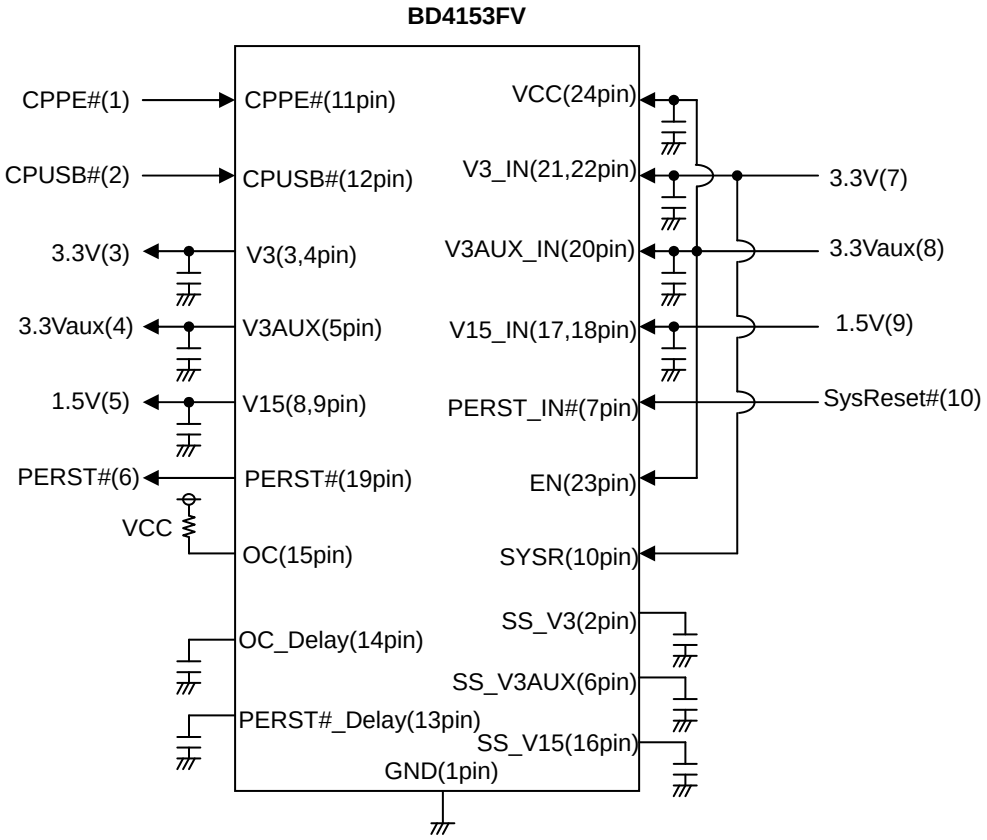
Mid Layer 2



Bottom Layer



●Appication Circuit (Circuit for ExpressCard™ Compliance Checklist)



●About heat loss

In designing heat, operate the apparatus within the following conditions.
(Because the following temperatures are warranted temperature, be sure to take margin, etc. into account.)

1. Ambient temperature Ta shall be not more than 125°C.
2. Chip junction temperature Tj shall be not more than 150°C.

Chip junction temperature Tj can be considered under the following two cases.

①Chip junction temperature Tj is found from IC surface temperature TC under actual application conditions:Tj=TC+θj-c×W
＜Reference value＞

θj-c:SSOP-B24	33℃/W	
HTSSOP-B24	36℃/W	

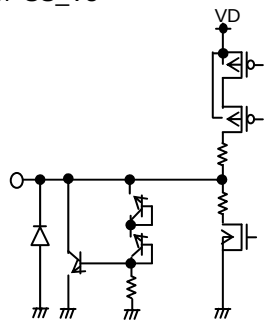
②Chip junction temperature Tj is found from ambient temperature Ta:Tj=TC+θj-a×W
＜Reference value＞

θj-a:SSOP-B24	243.9℃/W	(IC only)
	147.1℃/W	Single-layer substrate (substrate surface copper foil area: less 3%)
θj-a:HTSSOP-B24	113.6℃/W	Single-layer substrate (substrate surface copper foil area: less 3%)
	73.5℃/W	Double-layer substrate (substrate surface copper foil area:15×15mm^2)
	44.6℃/W	Double-layer substrate (substrate surface copper foil area: 70×70mm^2)
	31.3℃/W	Fourth-layer substrate (substrate surface copper foil area: 70×70mm^2)

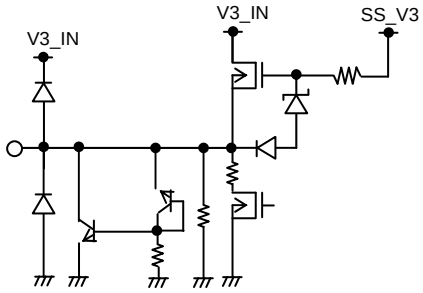
Most of heat loss in BD4153FV occurs at the output switch. The power lost is determined by multiplying the on-resistance by the square of output current of each switch. As BD4153EFV employs the power PKG, the thermal derating characteristics significantly depends on the pc board conditions. When designing, care must be taken to the size of a pc board to be used.

●Equivalent Circuit

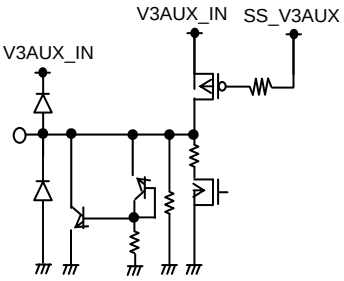
2pin<SS_V3>



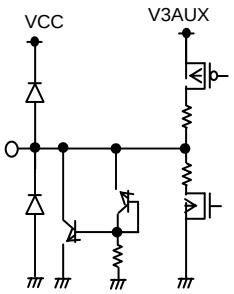
3,4pin<V3_1,V3_2>



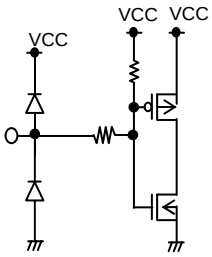
5pin<V3AUX>



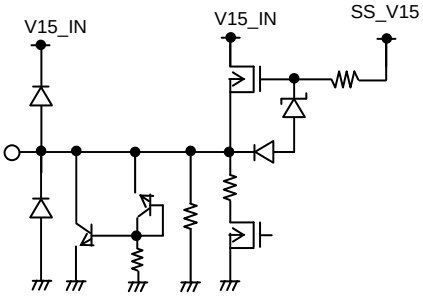
6pin<SS_V3AUX>



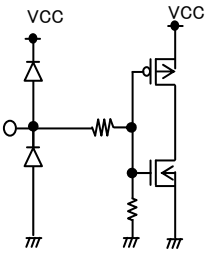
7pin<PERST_IN#>



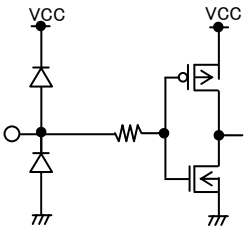
8,9pin<V15_1,V15_2>



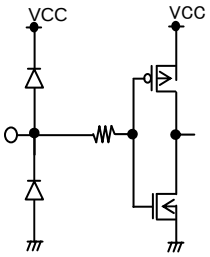
10pin<SYSR>



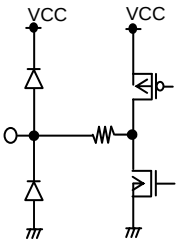
11pin<CPPE#>



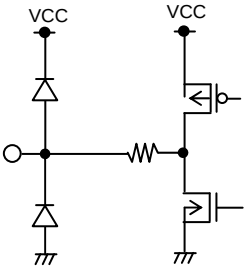
12pin<CPUSB#>



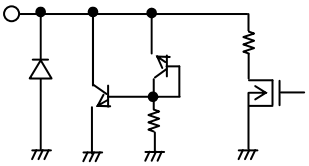
13pin<PERST#_DELAY>



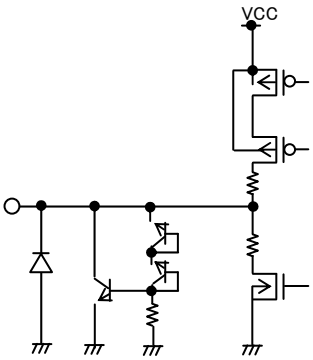
14pin<OC_DELAY>



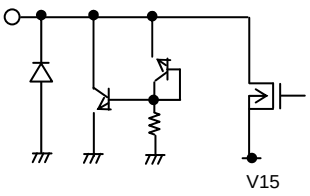
15pin<OC>



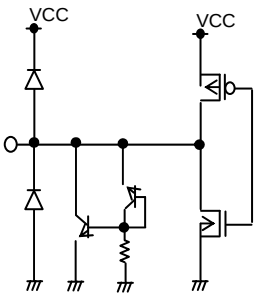
16pin<SS_V15>



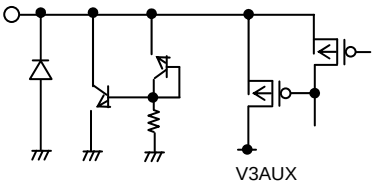
17,18pin<V15_IN1,V15_IN2>



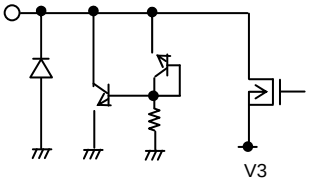
19pin<PERST#>



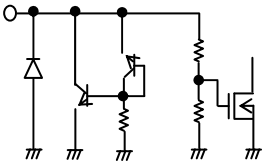
20pin<V3AUX_IN>



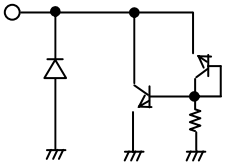
21,22pin<V3_IN1,V3_IN2>



23pin<EN >



24pin<VCC>



●Note For Use

1.Absolute maximum ratings

For the present product, thoroughgoing quality control is carried out, but in the event that applied voltage, working temperature range, and other absolute maximum rating are exceeded, the present product may be destroyed. Because it is unable to identify the short mode, open mode, etc., if any special mode is assumed, which exceeds the absolute maximum rating, physical safety measures are requested to be taken, such as fuses, etc.

2.GND potential

Bring the GND terminal potential to the minimum potential in any operating condition.

3.Thermal design

Consider allowable loss (Pd) under actual working condition and carry out thermal design with sufficient margin provided.

4.Terminal-to-terminal short-circuit and erroneous mounting

When the present IC is mounted to a printed circuit board, take utmost care to direction of IC and displacement. In the event that the IC is mounted erroneously, IC may be destroyed. In the event of short-circuit caused by foreign matter that enters in a clearance between outputs or output and power-GND, the IC may be destroyed.

5.Operation in strong electromagnetic field

The use of the present IC in the strong electromagnetic field may result in maloperation, to which care must be taken.

6.Built-in thermal shutdown protection circuit

The present IC incorporates a thermal shutdown protection circuit (TSD circuit). The working temperature is 175°C (standard value) and has a -15°C (standard value) hysteresis width. When the IC chip temperature rises and the TSD circuit operates, the output terminal is brought to the OFF state. The built-in thermal shutdown protection circuit (TSD circuit) is first and foremost intended for interrupt IC from thermal runaway, and is not intended to protect and warrant the IC. Consequently, never attempt to continuously use the IC after this circuit is activated or to use the circuit with the activation of the circuit premised.

7.Capacitor across output and GND

In the event a large capacitor is connected across output and GND, when Vcc and VIN are short-circuited with 0V or GND for some kind of reasons, current charged in the capacitor flows into the output and may destroy the IC. Use a capacitor smaller than 1000 μF between output and GND.

8.Inspection by set substrate

In the event a capacitor is connected to a pin with low impedance at the time of inspection with a set substrate, there is a fear of applying stress to the IC. Therefore, be sure to discharge electricity for every process. As electrostatic measures, provide grounding in the assembly process, and take utmost care in transportation and storage. Furthermore, when the set substrate is connected to a jig in the inspection process, be sure to turn OFF power supply to connect the jig and be sure to turn OFF power supply to remove the jig.

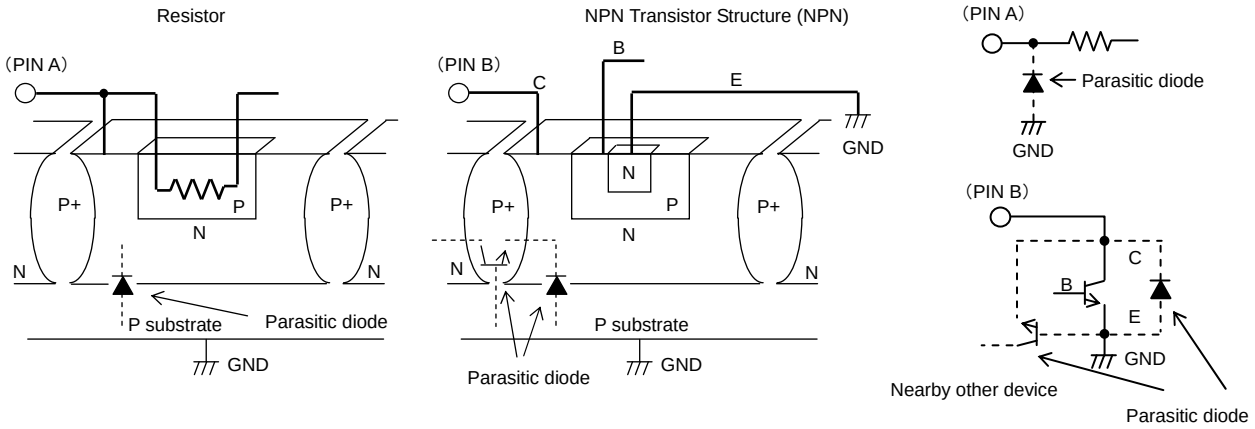
9.IC terminal input

The present IC is a monolithic IC and has a P substrate and P^+ isolation between elements.

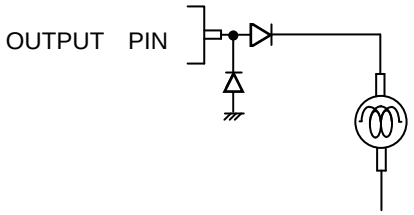
With this P layer and N layer of each element, PN junction is formed, and when the potential relation is

- GND>terminal A>terminal B, PN junction works as a diode, and
- terminal B>GND terminal A, PN junction operates as a parasitic transistor.

The parasitic element is inevitably formed because of the IC construction. The operation of the parasitic element gives rise to mutual interference between circuits and results in malfunction, and eventually, breakdown. Consequently, take utmost care not to use the IC to operate the parasitic element such as applying voltage lower than GND (P substrate) to the input terminal.



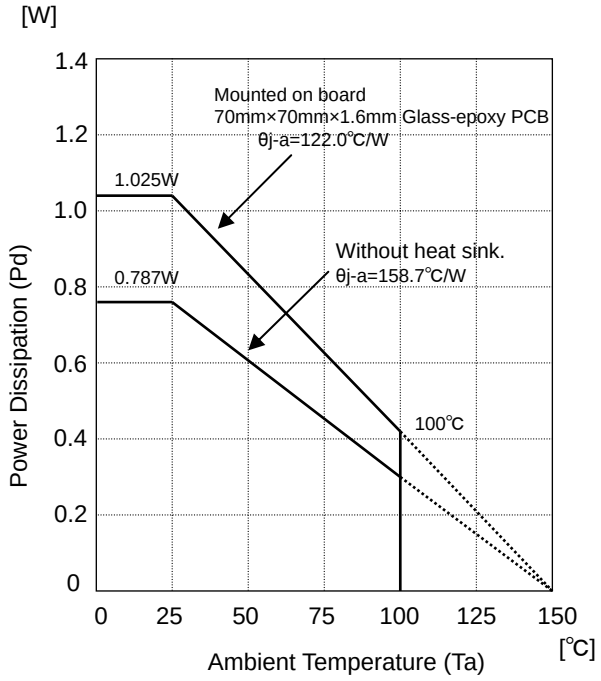
10. GND wiring pattern
    If there are a small signal GND and a high current GND, it is recommended to separate the patterns for the high current GND and the small signal GND and provide a proper grounding to the reference point of the set not to affect the voltage at the small signal GND with the change in voltage due to resistance component of pattern wiring and high current. Also for GND wiring pattern of component externally connected, pay special attention not to cause undesirable change to it.
11. Electrical characteristics
    The electrical characteristics in the Specifications may vary depending on ambient temperature, power supply voltage, circuit(s) externally applied, and/or other conditions. It is therefore requested to carefully check them including transient characteristics.
12. Capacitors to be applied to the input terminals
    The capacitors to be applied to the input terminals (VCC, V3_IN, V3AUX_IN and V15_IN) are used to lower the output impedance of the power supply to be connected. An increase in the output impedance of the power supply may result in destabilization of input voltages (VCC, V3_IN, V3AUX_IN and V15_IN). It is recommended to use a low ESR capacitor with less temperature coefficient (change in capacitance vs. change in temperature), 0.1 µF more or less for VCC and V3AUX_IN while 1 µF more or less for V3_IN and V15_IN, but it must be thoroughly checked at the temperature and with the load of the range expected to use because it significantly depends on the characteristics of the input power supply to be used and the conductor pattern of the pc board.
13. Capacitors to be applied to the output terminals
    To the output terminals (V3, V3_AUX, and V15), the output capacitors should be connected between the respective output terminal and GND. It is recommended to use a low ESR capacitor with less temperature coefficient, 1 µF more or less for V3 and V15 terminals while 1µF more or less for V3_AUX, but it must be thoroughly checked at the temperature and with the load of the range expected to use because it significantly depends on the temperature and the load conditions.
14. Not of a radiation-resistant design.
15. .Allowable loss Pd
    With respect to the allowable loss, the thermal derating characteristics are shown in the Exhibit, which we hope would be used as a good-rule-of-thumb. Should the IC be used in such a manner to exceed the allowable loss, reduction of current capacity due to chip temperature rise, and other degraded properties inherent to the IC would result. You are strongly urged to use the IC within the allowable loss.
16. In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.



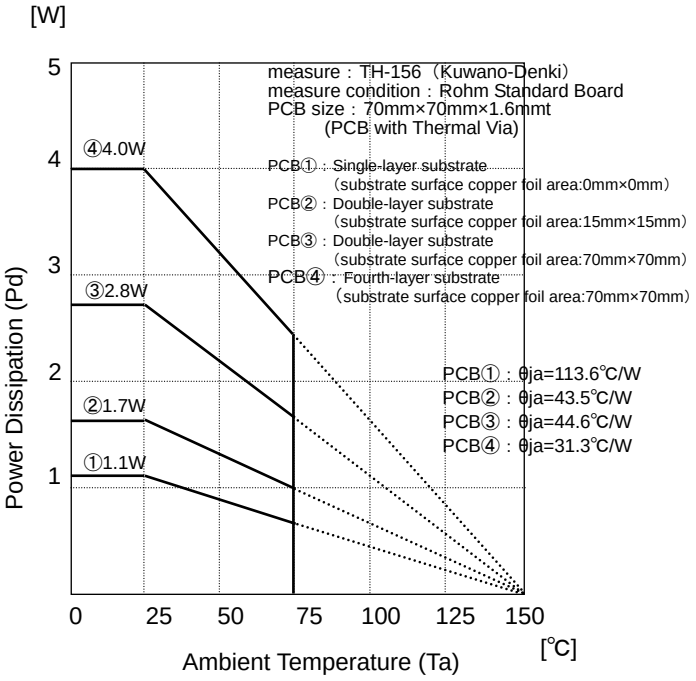
17. Operating ranges
    If it is within the operating ranges, certain circuit functions and operations are warranted in the working ambient temperature range. With respect to characteristic values, it is unable to warrant standard values of electric characteristics but there are no sudden variations in characteristic values within these ranges.
18. We are certain that examples of applied circuit diagrams are recommendable, but you are requested to thoroughly confirm the characteristics before using the IC.In addition, when the IC is used with the external circuit changed, decide the IC with sufficient margin providedwhile consideration is being given not only to static characteristics but also variations of external parts and our IC including transient
19. Wiring to the input terminals (V3 IN, V3AUX IN, and V15 IN) and output terminals (V3, V3AUX and V15) of built-in FET should be carried out with special care. Unnecessarily long and/or thin conductors used in wiring may result in degradation of characteristics including decrease in output voltage.
20. Heatsink
    Heatsink is connected to SUB, which should be short-circuited to GND. Solder the heatsink to a pc board properly, which offers lower thermal resistance.

●Power Dissipation

◎BD4153FV



◎BD4153EFV

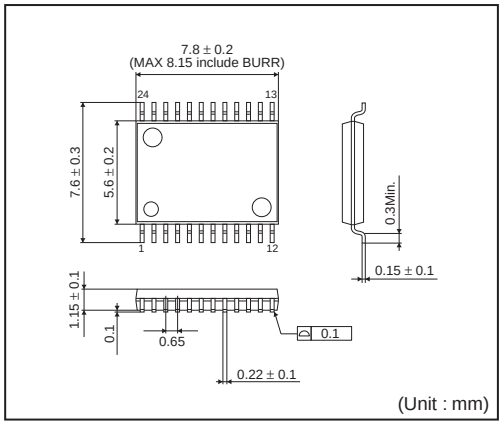


●Ordering part number

B	D	4	1	5	3	F	V	-	E	2

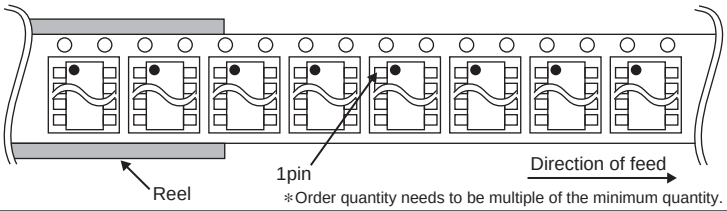
- BD: Part Number
- 4153: Part Number
- FV : SSOP-B24
  EFV : HTSSOP-B24
  Package
- E2: Embossed tape and reel (SSOP-B24/ HTSSOP-B24)
  Packaging and forming specification

SSOP-B24



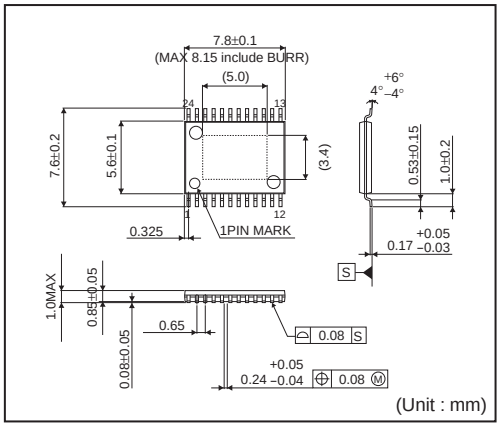
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



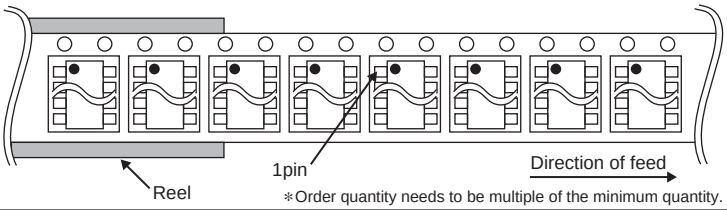
∗Order quantity needs to be multiple of the minimum quantity.

HTSSOP-B24



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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