

Vishay Siliconix

N-Channel 200-V (D-S) MOSFET

PRODUCT SUMMARY								
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A) ^a	Q _g (Typ.)					
200	1.38 at V _{GS} = 4.5 V	2.6						
	1.50 at V _{GS} = 2.5 V	2.5	5 nC					
	3.50 at V _{GS} = 1.8 V	0.5						

FEATURES

- Halogen-free
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package

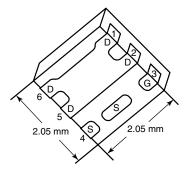
Boost Converter for Portable Devices

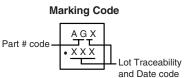
- Small Footprint Area
- Low On-Resistance

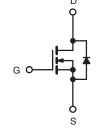
APPLICATIONS



PowerPAK SC-70-6L-Single







Ordering Information: SiA456DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted								
Parameter		Symbol	Limit	Unit				
Drain-Source Voltage		V_{DS}	200	V				
Gate-Source Voltage		V_{GS}	± 16	v				
	T _C = 25 °C		2.6					
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 70 °C	l _D	2.1	1				
Continuous Drain Current (1) = 130 °C)	T _A = 25 °C		1.1 ^{b, c}	1				
	T _A = 70 °C		0.9 ^{b, c}	Α				
Pulsed Drain Current		I _{DM}	2					
Continuous Source-Drain Diode Current	T _C = 25 °C		3.6					
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	2.9 ^{b, c}					
	T _C = 25 °C		19					
Maximum Power Dissipation	T _C = 70 °C	P _D	12	w				
Maximum Tower Dissipation	T _A = 25 °C	, р	3.5 ^{b, c}	7 "				
	T _A = 70 °C		2.2 ^{b, c}					
Operating Junction and Storage Temperature	Range	T _J , T _{stg}	- 55 to 150	°C				
Soldering Recommendations (Peak Tempera	ature) ^{d, e}		260	1				

THERMAL RESISTANCE RATINGS									
Parameter		Symbol	Typical	Maximum	Unit				
Maximum Junction-to-Ambient ^{b, f}	sient ^{b, f} $t \le 5$ s R_{thJA} 28 36		36	°C/W					
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	5.3	6.5] O/W				

Notes:

- b. Surface Mounted on 1" x 1" FR4 board.
- d. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 80 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static	-					
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	200			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$			265		
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	- I _D = 250 μA		- 3.5		mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	0.6		1.4	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 16 \text{ V}$			± 100	nA
		V _{DS} = 200 V, V _{GS} = 0 V			1	μΑ
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 200 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	2			Α
	, ,	V _{GS} = 4.5 V, I _D = 0.75 A		1.08	1.38	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 2.5 V, I _D = 0.5 A		1.12	1.5	Ω
	, ,	V _{GS} = 1.8 V, I _D = 0.1 A		1.2	3.5	
Forward Transconductance ^a	ward Transconductance ^a 9 _{fs}			5		S
Dynamic ^b		-		l	l	l
Input Capacitance						
Output Capacitance	C _{oss}	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz		12		pF
Reverse Transfer Capacitance	C _{rss}			6		
·		V _{DS} = 100 V, V _{GS} = 10 V, I _D = 1.1 A		9.5	14.5	nC
Total Gate Charge	Q_g			5	7.5	
Gate-Source Charge	Q _{gs}	$V_{DS} = 100 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 1.1 \text{ A}$		0.7		
Gate-Drain Charge	Q_{gd}			1.7		
ate Resistance R _g		f = 1 MHz		2		Ω
Turn-On Delay Time	t _{d(on)}			10	15	
Rise Time	t _r	$V_{DD} = 100 \text{ V, R}_{I} = 111 \Omega$		25	40	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 0.9 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_q = 1 \Omega$		30	45	
Fall Time	t _f	1D = 0.0 7, VGEN = 1.0 V, Vig = 1.22		20	30	no
Turn-On Delay Time	t _{d(on)}			5	10	ns -
Rise Time	t _r	V_{DD} = 100 V, R_{L} = 111 Ω		20	30	
Turn-Off Delay Time	t _{d(off)}	$V_{DD} = 100 \text{ V, } N_L = 111 \Omega$ $I_D \cong 0.9 \text{ A, } V_{GEN} = 10 \text{ V, } R_a = 1 \Omega$		16	25	
Fall Time	t _f	ID = 0.0 7, TGEN TO 1, TIG TE		12	20	
Drain-Source Body Diode Characteristic	s					
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			3.6	Α
Pulse Diode Forward Current	I _{SM}				2	
Body Diode Voltage	V_{SD}	$I_S = 0.9 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			40	80	ns
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 0.9 A, dI/dt = 100 A/μs, T _{.I} = 25 °C		40	80	nC
Reverse Recovery Fall Time	t _a	3.3 /s, απαι = 100 /νμ3, 1j = 20 0		21		nc
Reverse Recovery Rise Time	t _b			19		ns

Notes:

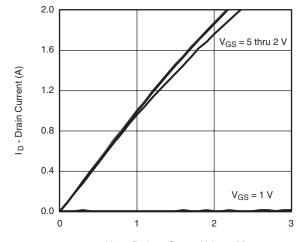
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 % b. Guaranteed by design, not subject to production testing.



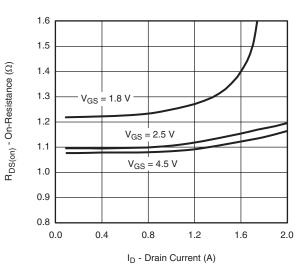
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

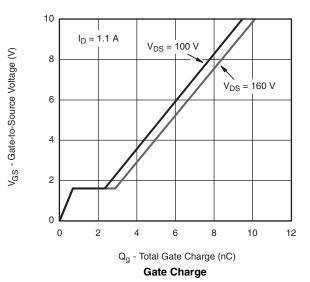


 V_{DS} - Drain-to-Source Voltage (V)

Output Characteristics

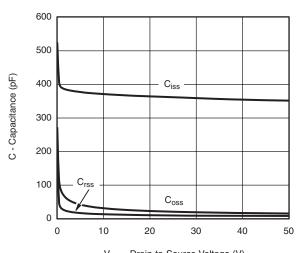


On-Resistance vs. Drain Current and Gate Voltage



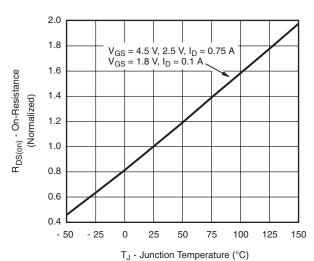
V_{GS} - Gate-to-Source Voltage (V)

Transfer Characteristics



 V_{DS} - Drain-to-Source Voltage (V)

Capacitance



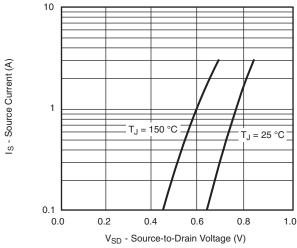
On-Resistance vs. Junction Temperature

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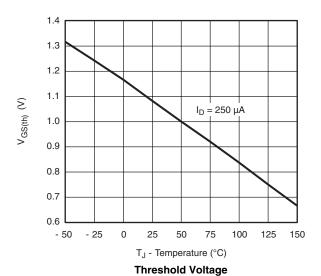
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



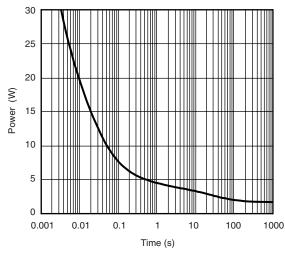
Source-Drain Diode Forward Voltage



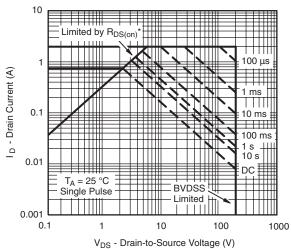
3.0 $I_D = 0.75 \text{ A}$ $I_D = 0$

V_{GS} - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power (Junction-to-Ambient)



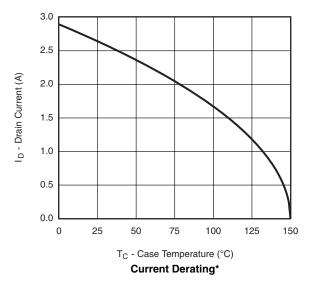
* V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified

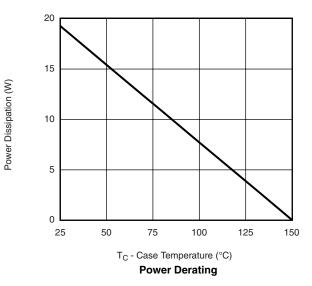
Safe Operating Area, Junction-to-Ambient



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





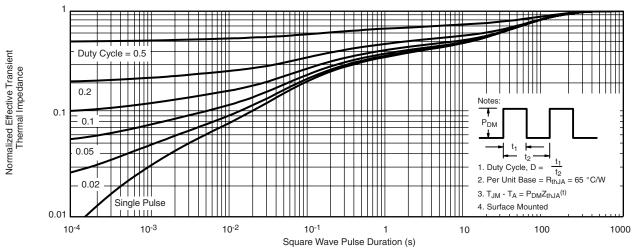
 $^{^*}$ The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?68642.





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PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
 Package outline exclusive of mold flash and metal burr
 Package outline inclusive of plating

	SINGLE PAD						DUAL PAD						
DIM	MILLIMETERS			INCHES			MILLIMETERS			INCHES			
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032	
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002	
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015	
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010	
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028	
D2	0.135	0.235	0.335	0.005	0.009	0.013							
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041	
E2	0.345	0.395	0.445	0.014	0.016	0.018							
E3	0.425	0.475	0.525	0.017	0.019	0.021							
е		0.65 BSC			0.026 BSC	;	0.65 BSC			0.026 BSC			
K		0.275 TYP			0.011 TYP		0.275 TYP		0.011 TYP				
K1		0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2		0.240 TYP		0.009 TYP		0.252 TYP		0.010 TYP					
К3		0.225 TYP		0.009 TYP					•	•			
K4		0.355 TYP		0.014 TYP									
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015	
T							0.05	0.10	0.15	0.002	0.004	0.006	

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DWG: 5934

06-Aug-07



RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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