XA1600E

Development Board Reference Manual

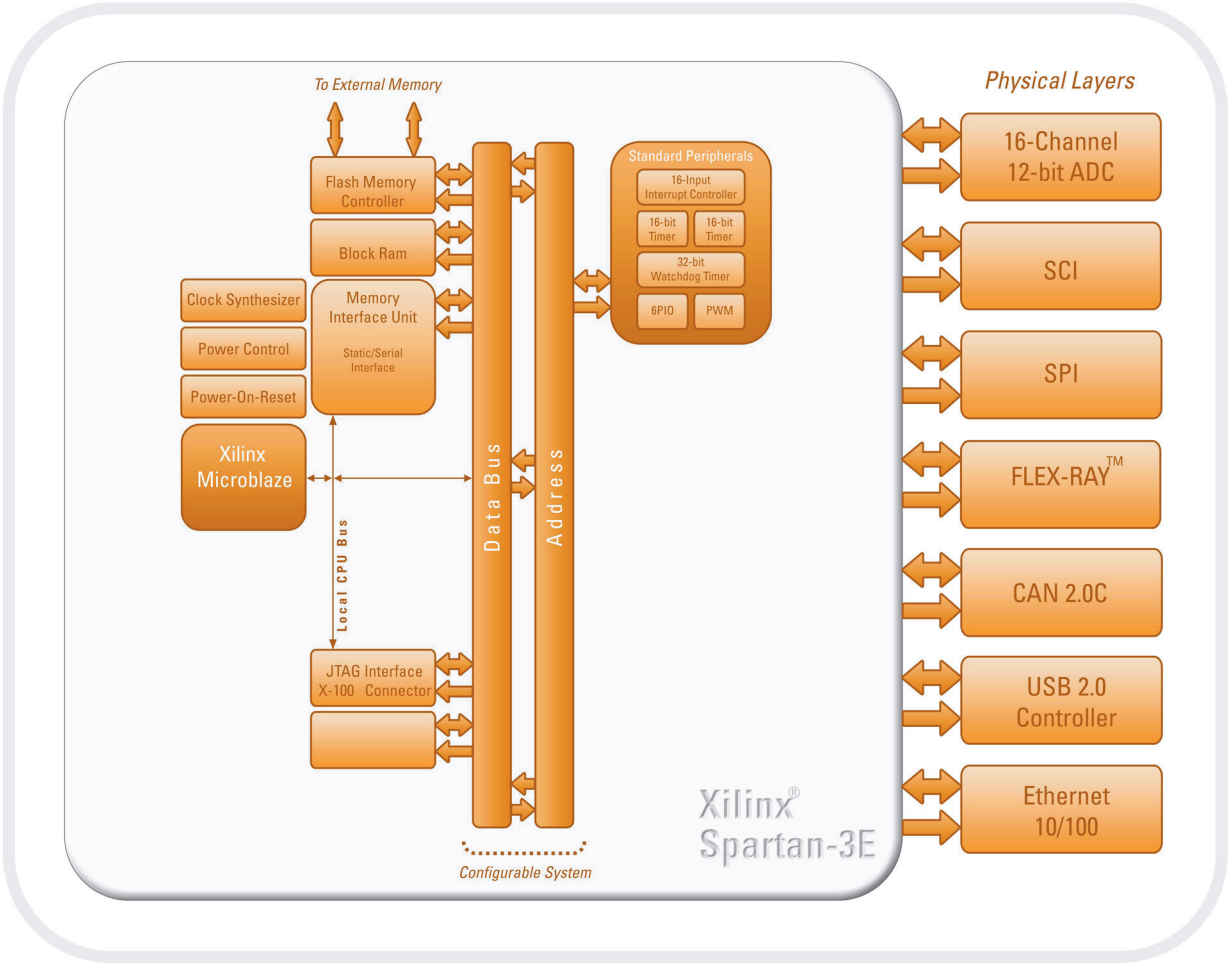
Contents

Introduction

Congratulations on your purchase of the Xilinx Automotive ECU Development kit including the XA1600E board designed by Si-Gate.
The XA1600E provides designers with a configurable ECU right out of the box suitable for a wide range of Automotive and Industrial applications. Please review the following reference manual thoroughly to receive the most of your new purchase.

The XA1600E is a complete 32-bit Field Configurable ECU platform, combining the highly popular Xilinx MicroBlaze™ processor core with standard System-on-Chip peripherals and over 150 user programmable I/O's. It is contained within a Xilinx Spartan-3A™ FPGA with programmable logic for custom driven IP
applications, a robust memory subsystem, and a full suite of Automotive and Industrial peripherals. The XA1600E enables programmable System-on-Chip applications and expands traditional development platforms by including necessary physical layers on-board the ECU. The XA1600E supports physical layers for 10/100 Ethernet, JTAG, USB 2.0, 12-bit ADC, High and Low Speed CAN, FlexRay™, LIN, K-Line, UART, and SPI along with on-board Flash and SRAM memory.

The XA1600E is ideal for projects where flexibility and expand-ability is needed for your future ECU developments.Please visit *www.xilinx.com/automotivekits* for additional or updated information which may not be presented in this manual.



*Block Diagram of the **Xilinx XA1600E** Field Configurable ECU*

XA1600E Memory Contents:

1). U140 XCF08 Configuration PROM 8MB
2). U650, U660 IDT71V416 SRAM 8MB(4MB x2)
3). U680, U690 MT28LC4M32B2-2 or EDS1232AATA-75 SDRAM 256M bits(128Mbit x2)
4). U640 M25P32VME Serial SPI 32Mbit (4M x 8)
5). U600,U610 JS28F320 FLASH 64Mbit (32Mbit x2)

Getting Started

The standard bit stream that is delivered with the Si-Gate XA1600E includes a Xilinx Microblaze Soft Core. This is integrated with a basic RS-232 demo application which provides the user the ability to immediately connect the XA1600E to a PC serial port and start developing. When coupled together with the Xilinx EDK tool-chain (must be purchased seperately) the XA1600E development kit provides everything the user needs to start writing software for Microblaze inside the Spar-tan-3 FPGA. If the user wants to develop new bit streams, this can be done with the purchase of the Xilinx ISE Foundation. Or the user may opt for a Si-Gate specialist to handle this integration task leaving room for the user to concentrate on their specific applications.

Communicating with the XA1600E

Because of the constant challenge in deciding which peripherals are needed in a new automotive system, several physical layers are included with the XA1600E which allow the user to add peripherals of their choice at any time without having to re-design the hardware interfaces including:

CAN 2.0C
ETHERNET 10/100 Part # LXT971 (Ethernet MAC needed inside FPGA for operation)
USB 2.0 Controller Part # CY7C68001
SPI
SCI
12 bit ADC

With the XA1600E's FPGA architecture, the user has the complete flexibility to select any combinations of automotive periphals, memory, and interface features that give the best system performance at the lowest costs on a single FPGA.

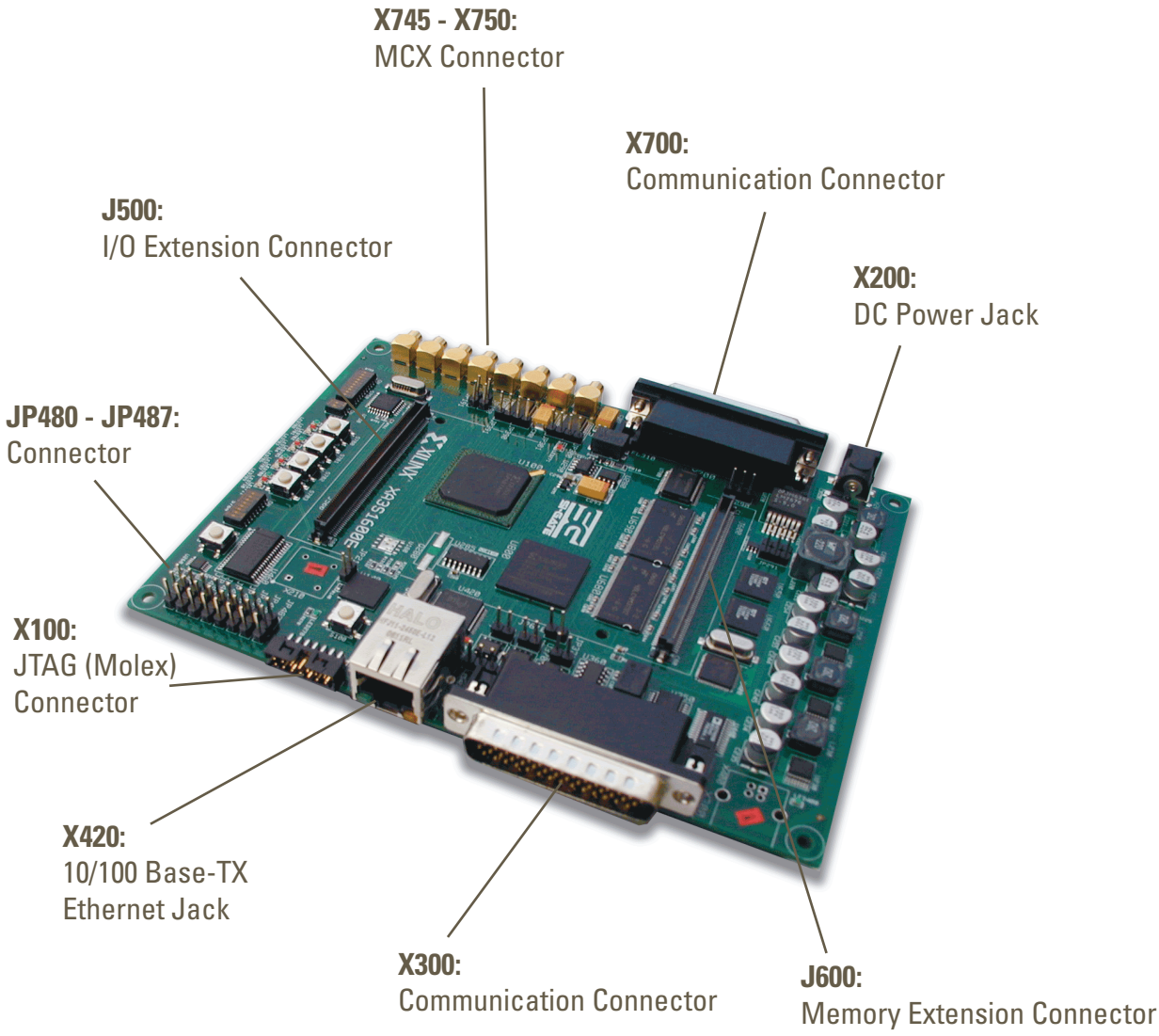
Xilinx MicroBlaze Soft Processor Core

The MicroBlaze core is a 3-stage pipeline 32-bit RISC Harvard architecture soft processor core with 32 general purpose registers, ALU, and rich instruction set optimized for embedded applications. It supports both on-chip block RAM and/or external memory.

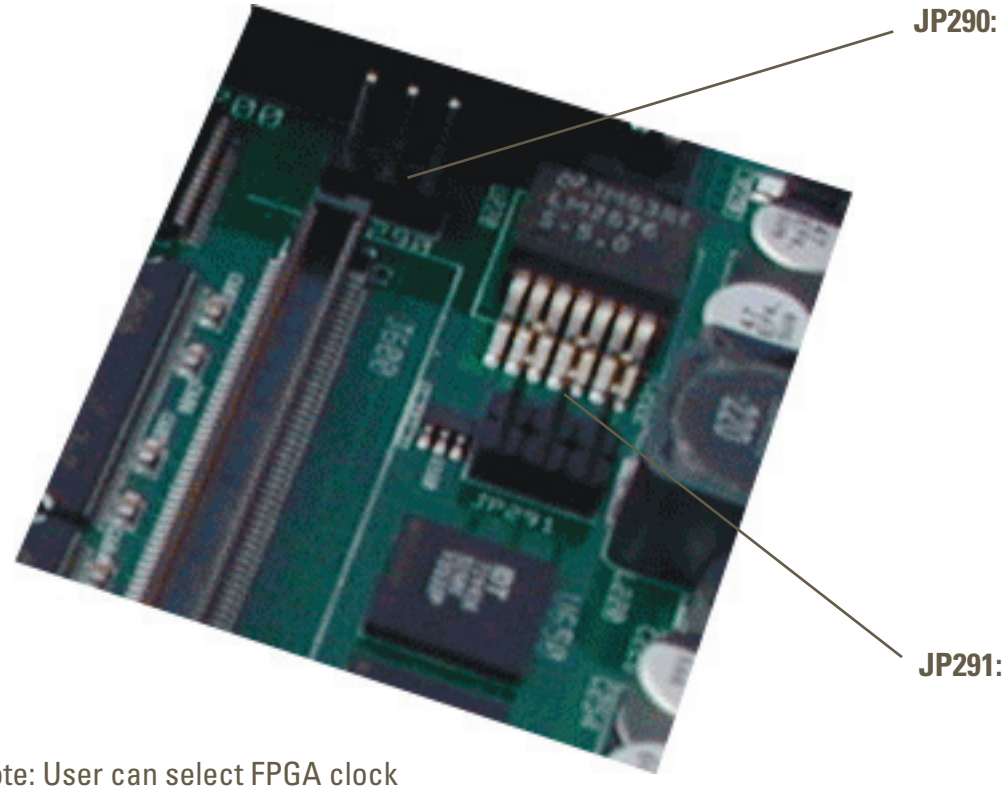
This basic design can then be configured with more advanced features such as: barrel shifter, floating-point unit (FPU), caches, exception handling, debug logic, and others. This flexibility allows the user to balance the required performance of the target application against the logic area cost of the soft processor. Additional information can be found at *www.xilinx.com* and *www.xilinx.com/automotivekits*.

Overview

The following section will inform you on the basic components of the XA1600E.



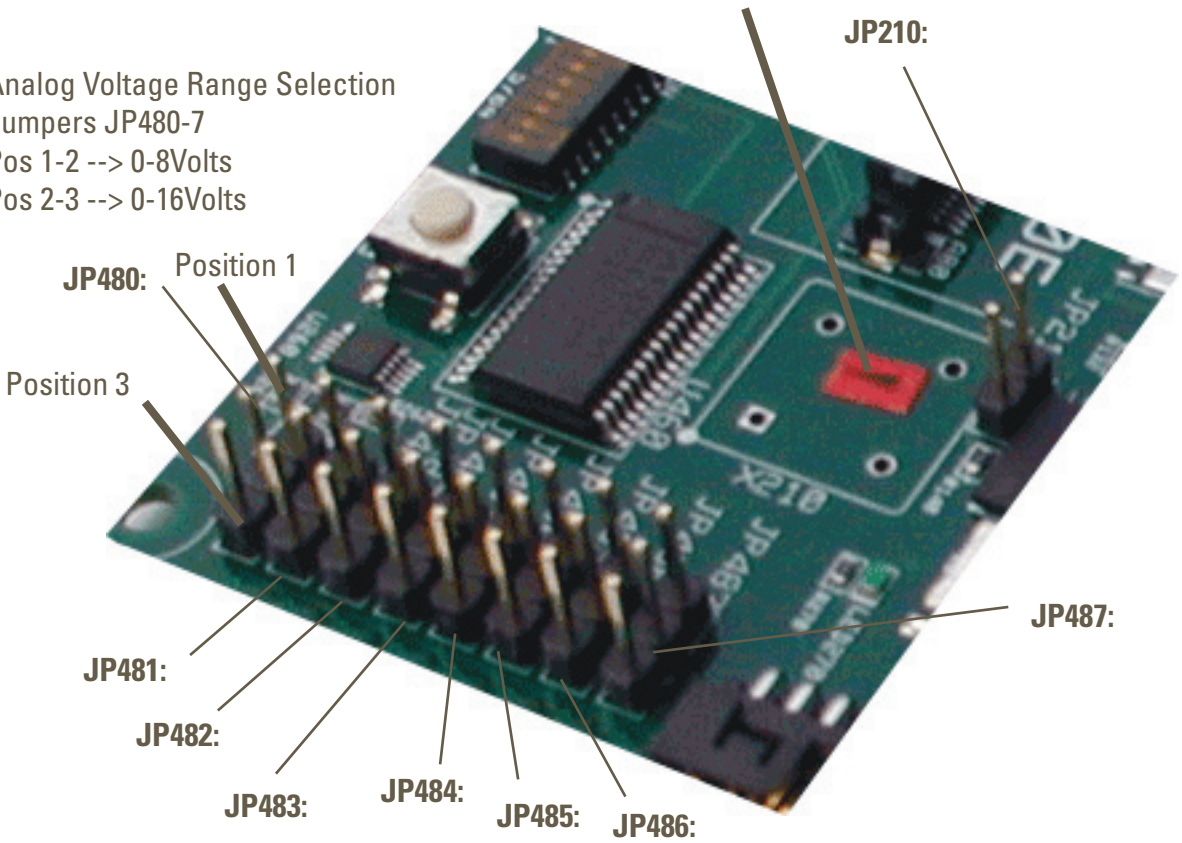
XA1600E User Interface	
X200: DC Power Jack (+12Volts Pos. Tip)	Connect the supplied mains adapter here
X700: Communication Connector	See pin out descriptions on page 11
X745-X750: SMA Connector	
J500: I/O Extension Connector	See pin out descriptions on page 13
X100: JTAG (Molex) Connector	
JP480 - JP 487:	Jumpers Selection for Analog Voltage Range Input Position 1-2 --> (0-8V) Position 2-3 --> (0-16V)
X420: 10/100 Base-TX Ethernet Jack	
X300: Communication Connector	See pin out descriptions on page 12
J600: I/O Extension Connector	See pin out descriptions on page 14

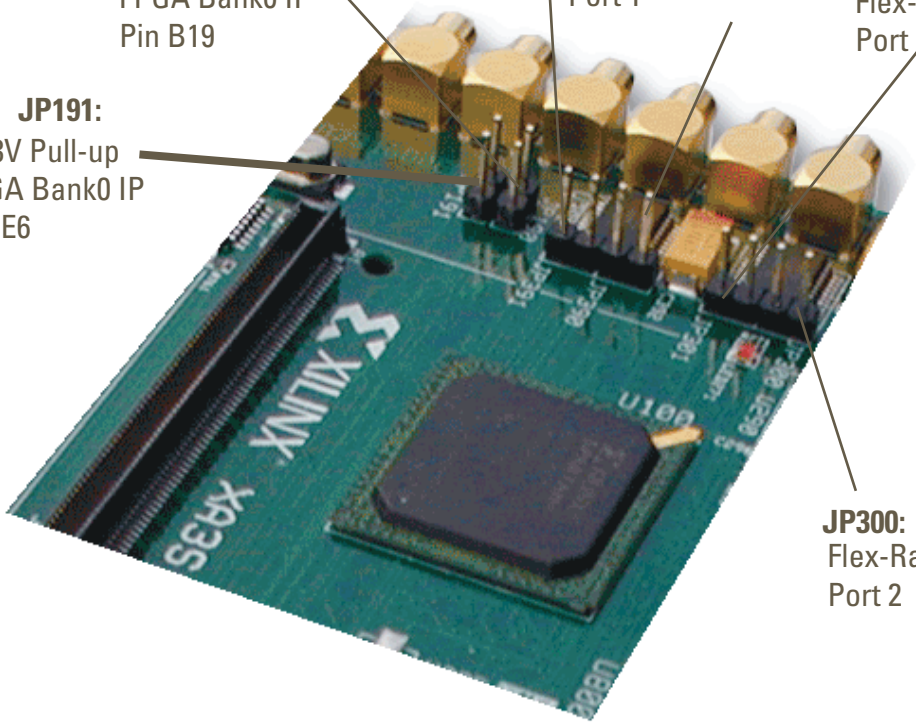


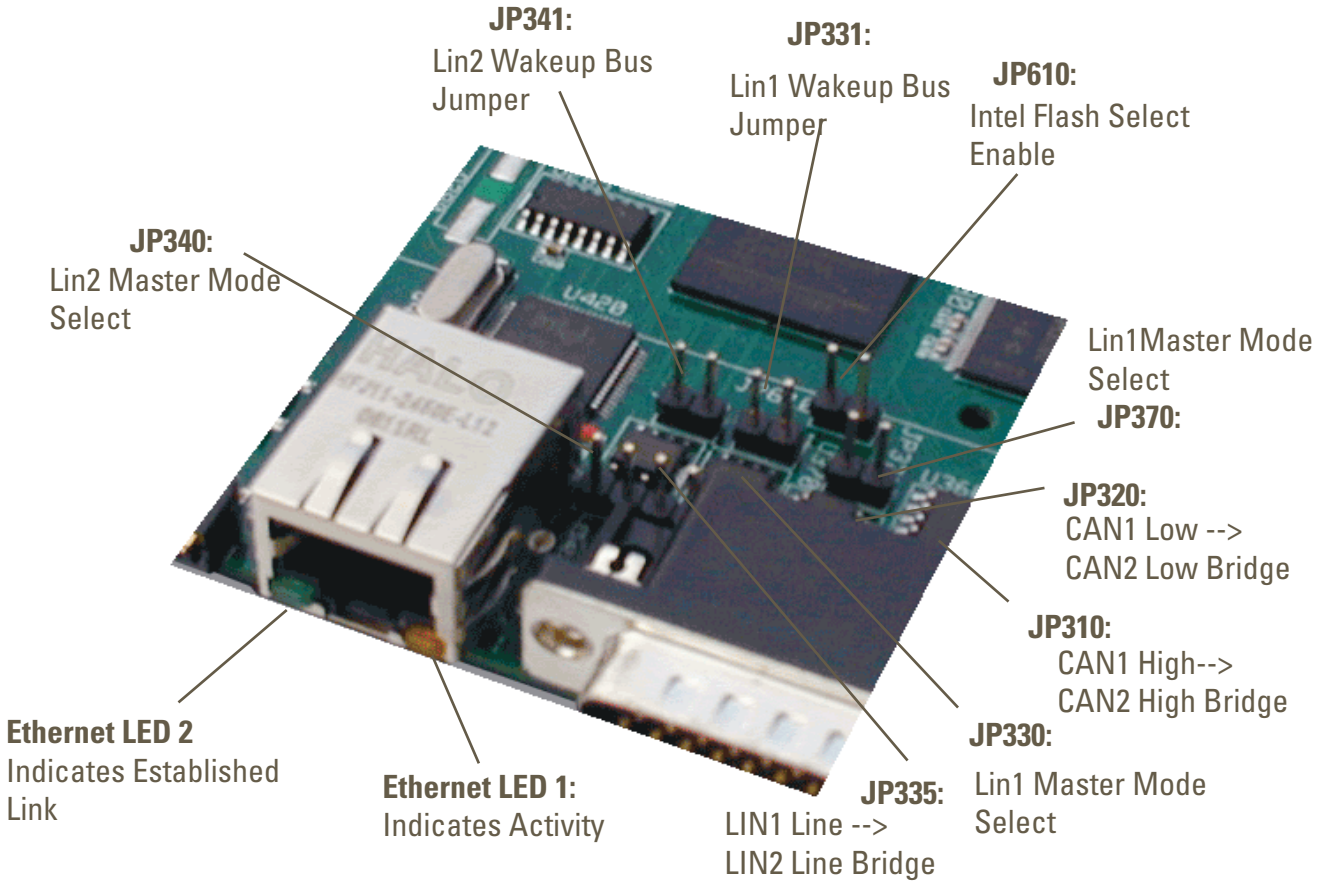
Note: User can select FPGA clock source from 24Mhz Y280 Crystal, Clock Synthesizer X750-1, X210 socket not shown, or external clk JP210. Refer to schematic PDF for FPGA Hookup.

X210 Crystal Socket not shown in photo

Analog Voltage Range Selection Jumpers JP480-7
Pos 1-2 --> 0-8Volts
Pos 2-3 --> 0-16Volts



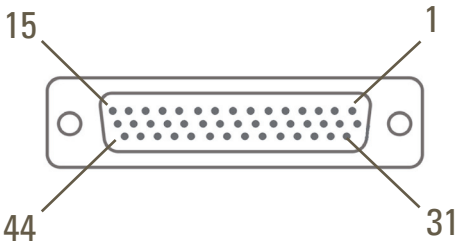

JP190:
+3.3V Pull-up
FPGA Bank0 IP
Pin B19
JP391:
JP390:
Flex-Ray Jumpers
Port 1
JP301:
Flex-Ray Jumper
Port 2
JP191:
+3.3V Pull-up
FPGA Bank0 IP
Pin E6
JP300:
Flex-Ray Jumper
Port 2


JP341:
Lin2 Wakeup Bus
Jumper
JP331:
Lin1 Wakeup Bus
Jumper
JP610:
Intel Flash Select
Enable
JP340:
Lin2 Master Mode
Select
Lin1Master Mode
Select
JP370:
JP320:
CAN1 Low -->
CAN2 Low Bridge
JP310:
CAN1 High-->
CAN2 High Bridge
Ethernet LED 2
Indicates Established
Link
Ethernet LED 1:
Indicates Activity
JP335:
LIN1 Line -->
LIN2 Line Bridge
JP330:
Lin1 Master Mode
Select

XA1600E LED's, Buttons, & Jump-	
Power LED	Indicates power is being supplied to the XA1600E
JP290:	
JP210:	
Reset LED: User or Power Fail Reset	Indicates power failure, power on or user reset
Config Done LED: FPGA Configured	Indicates that FPGA is configured
USBLED 400	Power active on USB socket
LED 392: User LED 1	User programmable LED 1
LED 393: User LED 2	User programmable LED 2
JP190:	+3.3V Pull-up FPGA Bank0 IP Pin B19
JP191:	Stuff to enable LIN2 master configuration
Ethernet LED 3	User programmable LED of ethernet PHY
S100:	Restart fpga configuration
S260: User Reset Button	Manual reset button
S700:	User programmable push button 1
S701:	User programmable push button 2
S702:	User programmable push button 3
S703:	User programmable push button 4
JP391:	Flex-Ray Jumper Port 1
JP390:	Flex-Ray Jumper Port 1
JP301:	Flex-Ray Jumper Port 2
JP300:	Flex-Ray Jumper Port 2
JP341:	Lin2 Wakeup Jumper
JP331:	Lin1 Wakeup Jumper
JP610:	Intel Flash Enable
JP370:	Lin Master Mode Select
Ethernet LED 1	User programmable LED of ethernet PHY (default shows activity)
Ethernet LED 2	User programmable LED of ethernet PHY (default shows link status)

Pin Out Descriptions

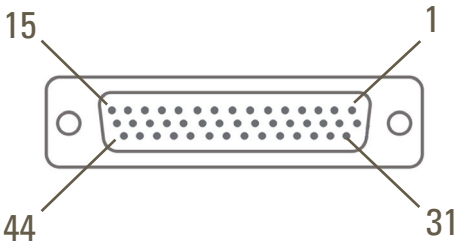
X700:
Communication Connector



Pin	Signal
1	CON_SG0
2	CON_SG1
3	CON_SG2
4	CON_SG3
5	CON_SG4
6	CON_SG5
7	CON_SG6
8	CON_SG7
9	CON_SG8
10	CON_SG9
11	CON_SG10
12	CON_SG11
13	CON_SG12
14	CON_SG13
15	CON_SP0
16	CON_SP1
17	CON_SP2
18	CON_SP3
19	CON_SP4
20	CON_SP5
21	CON_SP6
22	CON_SP7

Pin	Signal
23	CON_HSLS1
24	CON_HSLS2
25	CON_HSLS3
26	CON_HSLS4
27	CON_HSLS5
28	CON_HSLS6
29	CON_HSLS7
30	CON_HSLS8
31	FLEXRAY1 P
32	FLEXRAY1 M
33	FLEXRAY2 P
34	FLEXRAY2 M
35	IN CAN1 H
36	IN CAN1 L
37	+5V
38	VIGN
39	PGND
40	PGND
41	PGND
42	VBAT
43	VBAT
44	VBAT

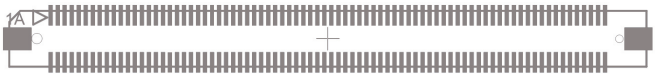
X300:
Communication Connector



Pin	Signal
1	LIN1 LINE
2	IN KLINE/LIN
3	GND
4	CANB H
5	IN CAN2 L
6	GND
7	RS2 RX
8	RS1 IX
9	GND
10	RS0 RX
11	ANA15
12	ANA13
13	ANA11
14	+2V5
15	+5V
16	LIN2 LINE
17	GND
18	OUT LLINE
19	CANB L
20	GND
21	IN CAN2 H
22	RS2 IX

Pin	Signal
23	GND
24	RS1 RX
25	RSO TX
26	GND
27	ANA14
28	ANA12
29	ANA10
30	+3V5
31	GNDA
32	GNDA
33	VDDA+5V
34	VDDA+5V
35	ANA9
36	ANA8
37	LS ANA7
38	LS ANA6
39	LS ANA5
40	LS ANA4
41	LS ANA3
42	LS ANA2
43	LS ANA1
44	LS ANA0

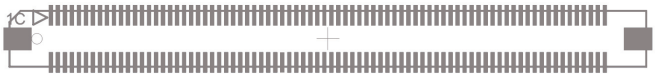
J500:
I/O Extension Connector



Signal	Pin	Pin	Signal
PA0	1A	1B	PC0
PA1	2A	2B	PC1
PA2	3A	3B	PC2
PA3	4A	4B	PC3
+3V3	5A	5B	GND
PA4	6A	6B	PC4
PA5	7A	7B	PC5
PA6	8A	8B	PC6
PA7	9A	9B	PC7
+3V3	10A	10B	GND
PA8	11A	11B	PC8
PA9	12A	12B	PC9
PA10	13A	13B	PC10
PA11	14A	14B	PC11
+3V3	15A	15B	GND
PA12	16A	16B	PC12
PA13	17A	17B	PC13
PA14	18A	18B	PC14
PA15	19A	19B	PC15
+3V3	20A	20B	GND
PA16	21A	21B	PC16
PA17	22A	22B	PC17
PA18	23A	23B	PC18
PA19	24A	24B	PC19
+3V3	25A	25B	GND
PA20	26A	26B	PC20
PA21	27A	27B	PC21
PA22	28A	28B	PC22
PA23	29A	29B	PC23
+3V3	30A	30B	GND
PA24	31A	31B	PC24
PA25	32A	32B	PC25
PA26	33A	33B	PC26
PA27	34A	34B	PC27
+3V3	35A	35B	GND
PA28	36A	36B	PC28
PA29	37A	37B	PC29
PA30	38A	38B	PC30
PA31	39A	39B	PC31
+3V3	40A	40B	GND

Signal	Pin	Pin	Signal
PB0	41A	41B	PD0
PB1	42A	42B	PD1
PB2	43A	43B	PD2
PB3	44A	44B	PD3
+1V2	45A	45B	GND
PB4	46A	46B	PD4
PB5	47A	47B	PD5
PB6	48A	48B	PD6
PB7	49A	49B	PD7
+1V2	50A	50B	GND
PB8	51A	51B	PD8
PB9	52A	52B	PD9
PB10	53A	53B	PD10
PB11	54A	54B	PD11
+1V2	55A	55B	GND
PB12	56A	56B	PD12
PB13	57A	57B	PD13
PB14	58A	58B	PD14
PB15	59A	59B	PD15
+1V2	60A	60B	GND
PB16	61A	61B	PD16
PB17	62A	62B	PD17
PB18	63A	63B	PD18
PB19	64A	64B	PD19
+1V2	65A	65B	GND
PB20	66A	66B	PD20
PB21	67A	67B	PD21
PB22	68A	68B	PD22
PB23	69A	69B	PD23
+1V2	70A	70B	GND
PB24	71A	71B	PD24
PB25	72A	72B	PD25
PB26	73A	73B	PD26
PB27	74A	74B	PD27
+1V2	75A	75B	GND
PB28	76A	76B	PD28
PB29	77A	77B	PD29
PB30	78A	78B	PD30
PB31	79A	79B	PD31
+1V2	80A	80B	GND

J600:
I/O Extension Connector



Signal	Pin	Pin	Signal
BD0	1C	1D	MEM_#RD
BD1	2C	2D	MEM_#OE
BD2	3C	3D	MEM_#WE
BD3	4C	4D	UNUSED
+5V	5C	5D	GND
BD4	6C	6D	MEM_#BE3
BD5	7C	7D	MEM_#BE2
BD6	8C	8D	MEM_#BE1
BD7	9C	9D	MEM_#BE0
+5V	10C	10D	GND
BD8	11C	11D	SRAM_#CS
BD9	12C	12D	FLASH_#CS
BD10	13C	13D	FLASH_#RP
BD11	14C	14D	FLASH_STS
+5V	15C	15D	GND
BD12	16C	16D	USB_#CS
BD13	17C	17D	USB_#RESET
BD14	18C	18D	USB_#IFCLK
BD15	19C	19D	USB_#INT
+5V	20C	20D	GND
BD16	21C	21D	USB_WAKEUP
BD17	22C	22D	USB_READY
BD18	23C	23D	USB_FLAGA
BD19	24C	24D	USB_FLAGB
+5V	25C	25D	GND
BD20	26C	26D	USB_FLAGC
BD21	27C	27D	USB_PKTEND
BD22	28C	28D	EXT1_#CS
BD23	29C	29D	SDRAM_#CS
+5V	30C	30D	GND
BD24	31C	31D	EXT_TDO
BD25	32C	32D	EXT_TDI
BD26	33C	33D	CFG_TMS
BD27	34C	34D	CFG_TCK
+5V	35C	35D	GND
BD28	36C	36D	BYPASS_#0E
BD29	37C	37D	+2V5
BD30	38C	38D	CFG DONE2
BD31	39C	39D	UNUSED
+5V	40C	40D	GND

Signal	Pin	Pin	Signal
BA31	41C	41D	SPI0_MISO
BA30	42C	42D	SPI0_MOSI
BA29	43C	43D	SPI0_SCLK
BA28	44C	44D	SPI1_#CS0
+2V5	45C	45D	GND
BA27	46C	46D	SPI1_#CS1
BA26	47C	47D	SPI1_#CS2
BA25	48C	48D	SPI0_#CS2
BA24	49C	49D	SPI0_#CS1
+2V5	50C	50D	GND
BA23	51C	51D	SPI0_#CSO
BA22	52C	52D	SPI0_SCLK
BA21	53C	53D	SPI0_MOSI
BA20	54C	54D	SPI0_MISO
+2V5	55C	55D	GND
BA19	56C	56D	UNUSED
BA18	57C	57D	USW EXT0
BA17	58C	58D	USWEXT1
BA16	59C	59D	USWEXT2
+2V5	60C	60D	GND
BA15	61C	61D	UNUSED
BA14	62C	62D	UNUSED
BA13	63C	63D	UNUSED
BA12	64C	64D	UNUSED
+2V5	65C	65D	GND
BA11	66C	66D	UNUSED
BA10	67C	67D	UNUSED
BA9	68C	68D	UNUSED
BA8	69C	69D	UNUSED
+2V5	70C	70D	GND
BA7	71C	71D	UNUSED
BA6	72C	72D	UNUSED
BA5	73C	73D	UNUSED
BA4	74C	74D	UNUSED
+2V5	75C	75D	GND
BA3	76C	76D	VSUPPLY
BA2	77C	77D	VSUPPLY
BA1	78C	78D	VSUPPLY
BA0	79C	79D	VSUPPLY
+2V5	80C	80D	GND

For more information about available IP cores to integrate on XA1600E platform please visit:

www.xilinx.com/automotivekits

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